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RENESAS

R0P7760TH001TRK

User's Manual

SH7760 T-Engine Development Kit

User's Manual

Renesas Technology
www.renesas.com

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Cautions

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Precautions for Safety

Definitions of Signal Words

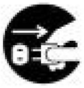
In both the user's manual and on the product itself, several icons are used to insure proper handling of this product and also to prevent injuries to you or other persons, or damage to your properties.
This chapter describes the precautions which should be taken in order to use this product safely and properly. Be sure to read this chapter before using this product.

	This symbol represents a warning about safety. It is used to arouse caution about a potential danger that will possibly inflict an injury on persons. To avoid a possible injury or death, please be sure to observe the safety message that follows this symbol.
⚠ **DANGER**	**DANGER** indicates an imminently dangerous situation that will cause death or heavy wound unless it is avoided. However, there are no instances of such danger for the product presented in this manual.
⚠ **WARNING**	**WARNING** indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.
⚠ **CAUTION**	**CAUTION** indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury unless it is avoided.
CAUTION	**CAUTION** with no safety warning symbols attached indicates a potentially dangerous situation that will cause property damage unless it is avoided.
IMPORTANT	This is used in operation procedures or explanatory descriptions to convey exceptional conditions or cautions to the user.

In addition to the five above, the following are also used as appropriate.

△means WARNING or CAUTION.
Example:  CAUTION AGAINST AN ELECTRIC SHOCK

⃠means PROHIBITION.
Example:  DISASSEMBLY PROHIBITED

●means A FORCIBLE ACTION.
Example:  UNPLUG THE POWER CABLE FROM THE RECEPTACLE.

⚠ WARNING

Warnings for AC Power Supply:

- If the attached AC power cable does not fit the receptacle, do not alter the AC power cable and do not plug it forcibly. Failure to comply may cause electric shock and/or fire.
- Use an AC power cable which complies with the safety standard of the country.
- Do not touch the plug of the AC power cable when your hands are wet. This may cause electric shock.
- This product is connected signal ground with frame ground. If your developing product is transformless (not having isolation transformer of AC power), this may cause electric shock. Also, this may give an unrepairable damage to this product and your developing one.
  While developing, connect AC power of the product to commercial power through isolation transformer in order to avoid these dangers.
- If other equipment is connected to the same branch circuit, care should be taken not to overload the circuit.
- When installing this equipment, insure that a reliable ground connection is maintained.
- If you smell a strange odor, hear an unusual sound, or see smoke coming from this product, then disconnect power immediately by unplugging the AC power cable from the outlet.
  Do not use this as it is because of the danger of electric shock and/or fire. In this case, contact your local distributor.
- Before setting up this product and connecting it to other devices, turn off power or remove a power cable to prevent injury or product damage.

Warnings to Be Taken for This Product:

- Do not disassemble or modify this product. Personal injury due to electric shock may occur if this product is disassembled and modified. Disassembling and modifying the product will void your warranty.
- Make sure nothing falls into the cooling fan on the top panel, especially liquids, metal objects, or anything combustible.

Warning for Installation:

- Do not set this product in water or areas of high humidity. Make sure that the product does not get wet. Spilling water or some other liquid into the product may cause unrepairable damage.

Warning for Use Environment:

- This equipment is to be used in an environment with a maximum ambient temperature of 35°C. Care should be taken that this temperature is not exceeded.

⚠ CAUTION
Note on Connecting the Power Supply: ● Do not use any power cable other than the one that is included with the product. ● The power cable included with the product has its positive and negative poles color-coded by red and black, respectively. ● Pay attention to the polarities of the power supply. If its positive and negative poles are connected in reverse, the internal circuit may be broken. ● Do not apply any voltages exceeding the product's rated power supply voltage (5.0 V ±5%). Extreme voltages may cause a burn due to abnormal heat or cause the internal circuit to break down.
Cautions to Be Taken for Handling This Product: ● Use caution when handling the main unit. Be careful not to apply a mechanical shock. ● Do not touch the connector pins of the product main unit and the target MCU connector pins directly. Static electricity may damage the internal circuits. ● Excessive flexing or force of the flexible cable for connecting this product to the emulation probe may break connector.
Cautions to Be Taken for System Malfunctions: ● If the product malfunctions because of interference like external noise, do the following to remedy the trouble. (1) Press the RESET button on the board. (2) If normal operation is not restored after step (1), shut OFF the product once and then reactivate it.

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User Registration

When you have purchased the product presented in this manual, please register your name and address. Your registered information is used for only after-sale services, and not for any other purposes. Without user registration, you will not be able to receive maintenance services such as a notification of field changes or trouble information. So be sure to register your name and address.
To get reference information about user registration, please visit the Web site shown below.

[Renesas Tools Homepage] http://www.renesas.com/en/tools/

[Inquiries] regist_tool@renesas.com

1. Outline

This chapter describes the package components, the system configuration and the preparation for using this product for the first time.

1.1 Package Components

The R0P7760TH001TRK package consists of the following items. When unpacking it, check to see if your R0P7760TH001TRK contains all of these items.

Table 1.1 Package components

Item		Quantity
T-Engine Board		1
ACadapter		1
RS-232C cable		1
CD-ROM	- T-Engine Board User’s Manual (This Manual) - T-Kernel and other software and various documentation (Personal Media Corporation)	1

* Please keep the R0P7760TH001TRK’s packing box and cushion material in your place for reuse at a later time when sending your product for repair or other purposes. Always use these packing box and cushion material when transporting this product.

* If there is any question or doubt about the packaged product, contact your local distributor.

1.2 System Configuration

1.2.1 T-Engine Features

The following summarizes the main features of T-Engine.

(1) The manual covers all information about T-Engine, including the circuit diagrams, connector specifications, and internal logic of FPGA employed on this board.

(2) The peripheral LSI chips (PCMCIA controller and sound generator chips) are commercially available.

(3) This board contains the PCMCIA controller, sound generator chip, SIM card connector, etc., so that application systems can be developed taking advantage of them.

(4) This board contains two SH7760 buses (address bus and data bus) and one extension slot subject to control signal output so that users can connect user-specific hardware.

1.2.2 T-Engine Configuration

Figure 1.1 shows a T-Engine Board system configuration and Figure 1.2 shows a T-Engine block diagram. Users must prepare any user-specific devices as needed, in addition to preparing the T-Engine and its accessories.

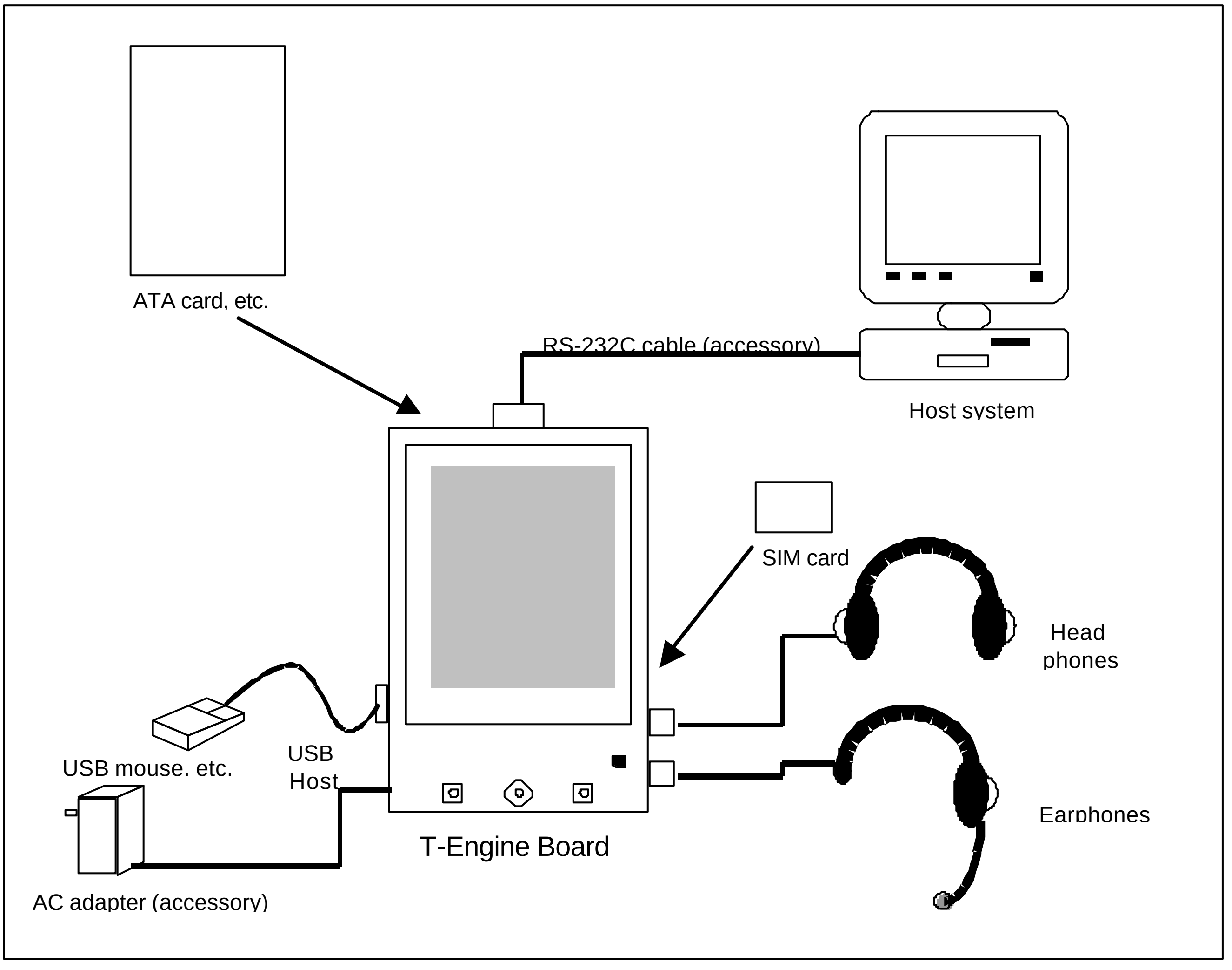


Figure 1.1 System configuration

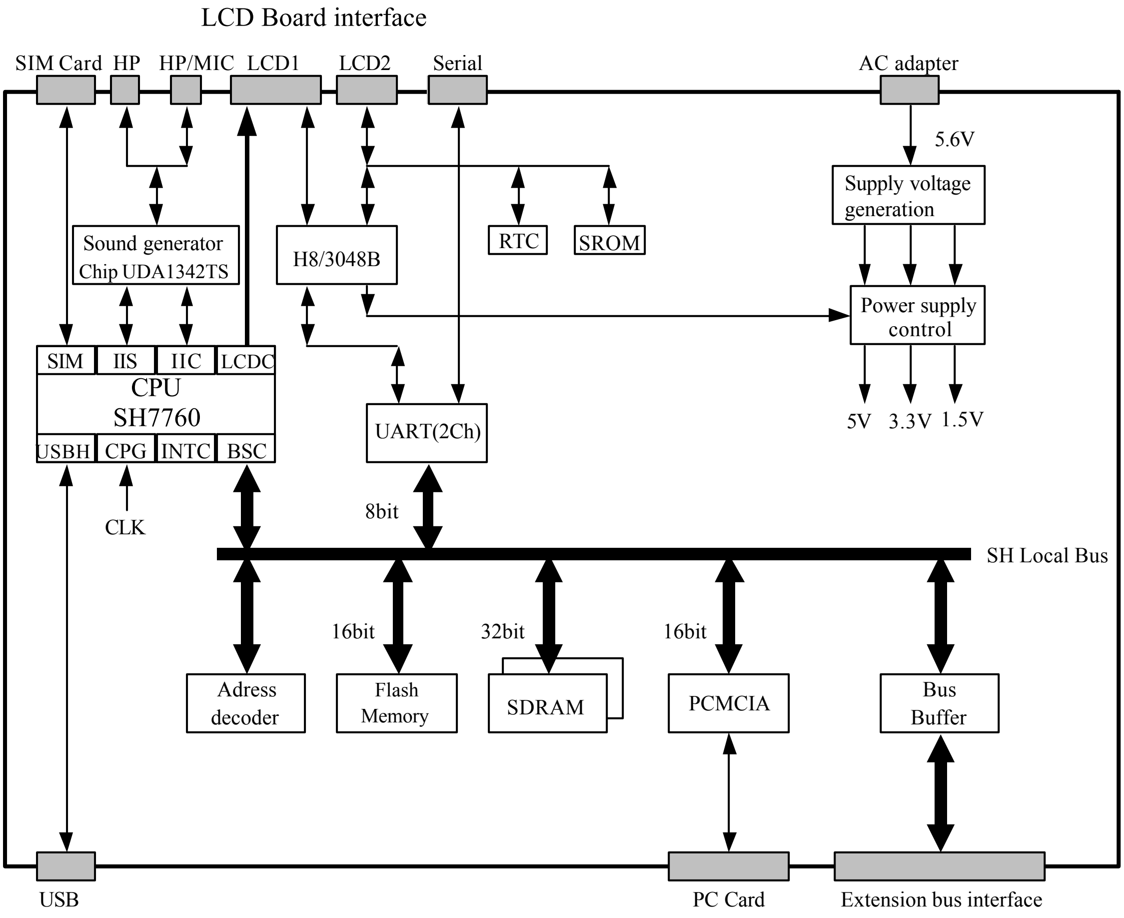


Figure 1.2 T-Engine Block Diagram

1.3 T-Engine Appearance

T-Engine Board consists of four boards: CPU, LCD, debug, and I/O boards. Figure 1.3 is an external view of the T-Engine. Figures 1.4 to 1.7 show the appearances of the respective boards (LCD, CPU, debug, and I/O boards).

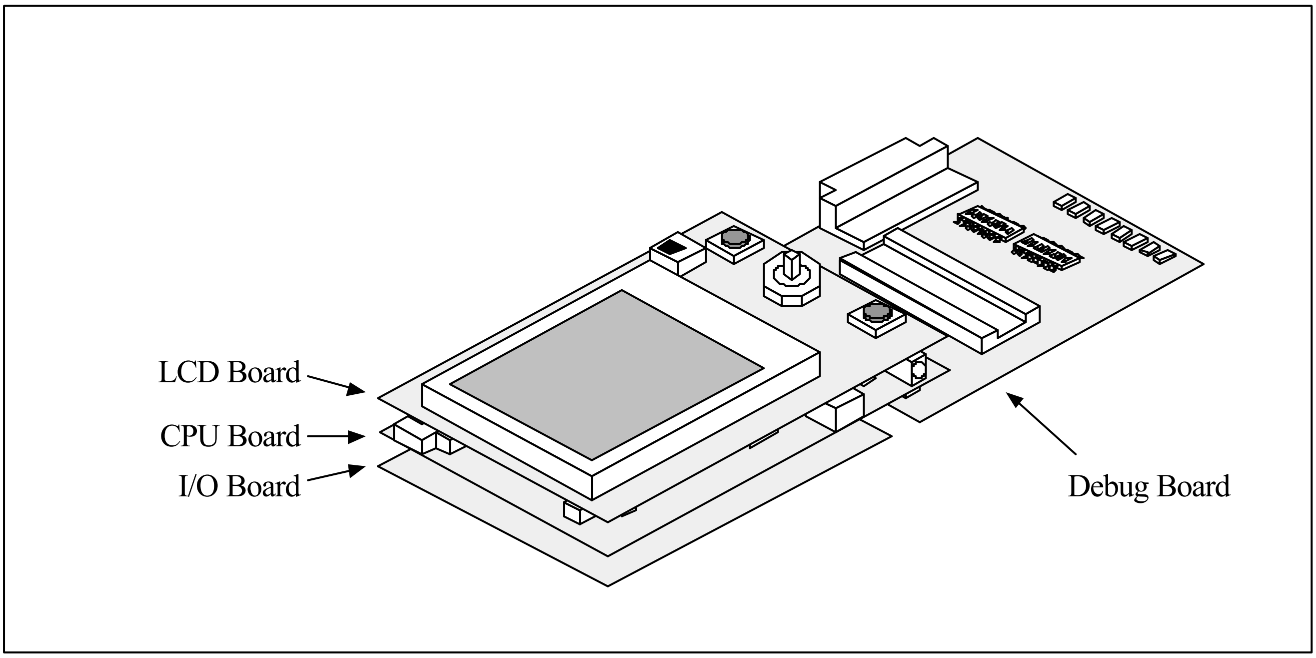


Figure 1.3 T-Engine - External View

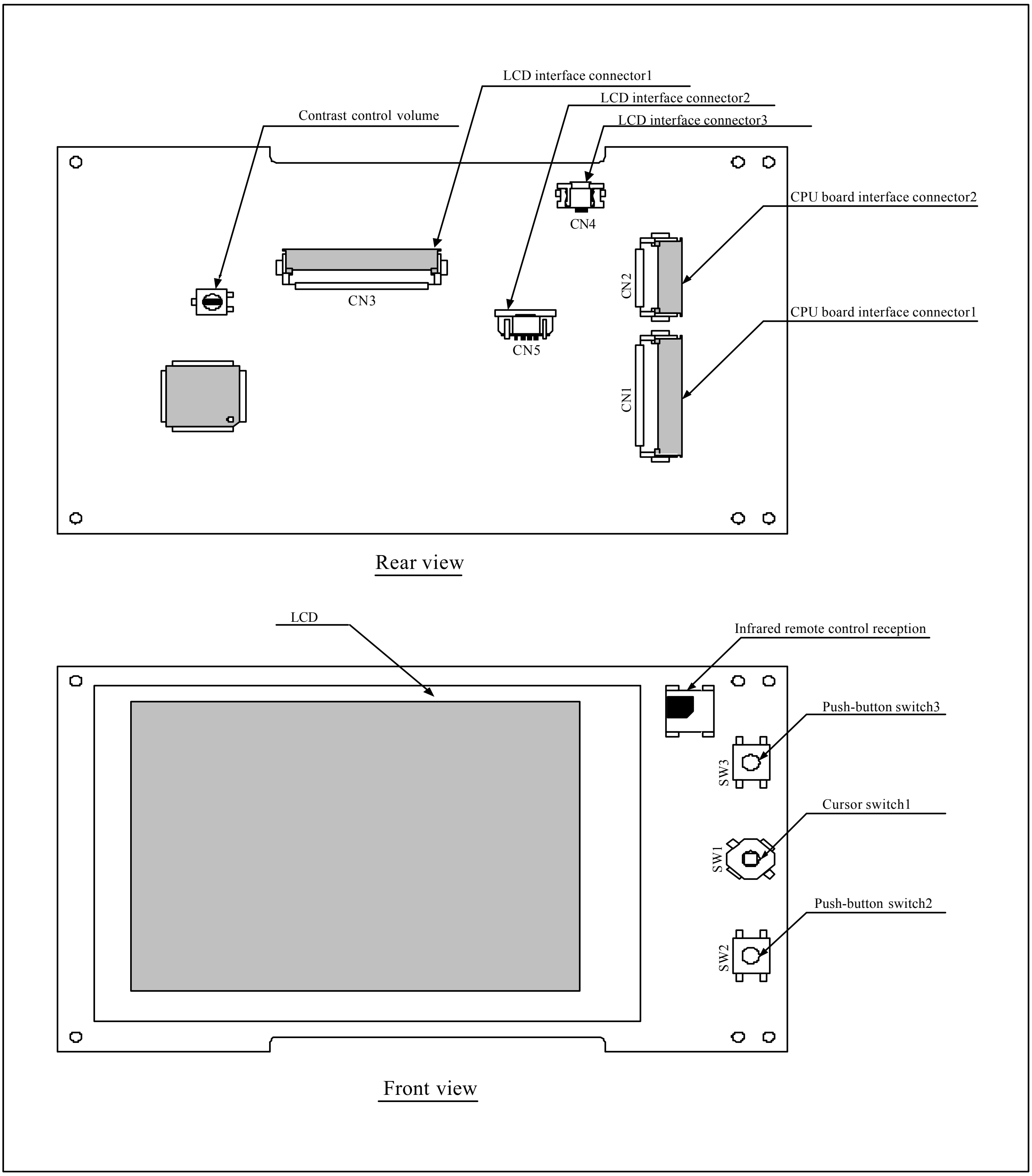


Figure 1.4 LCD Board - External View

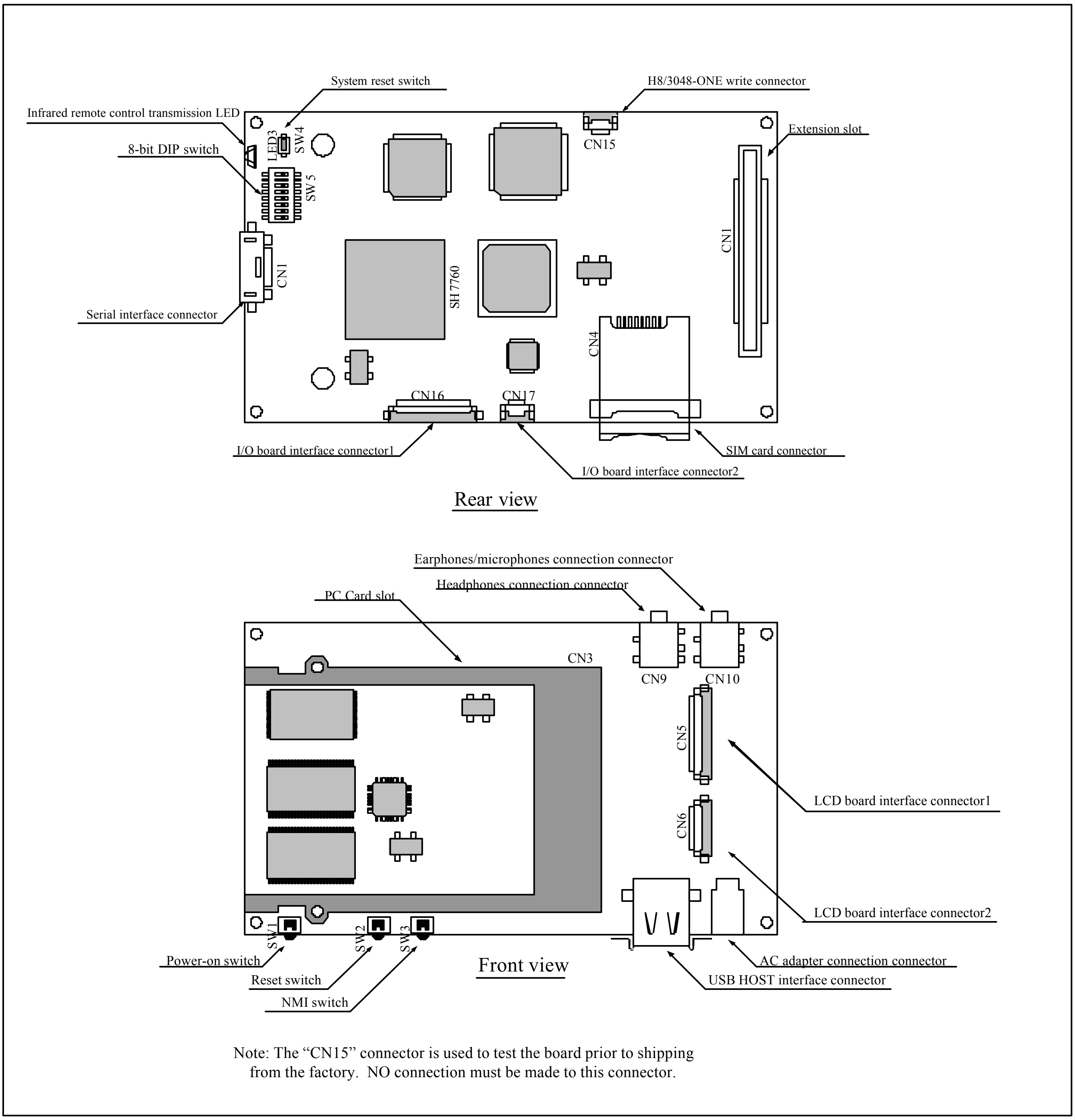


Figure 1.5 CPU Board - External View

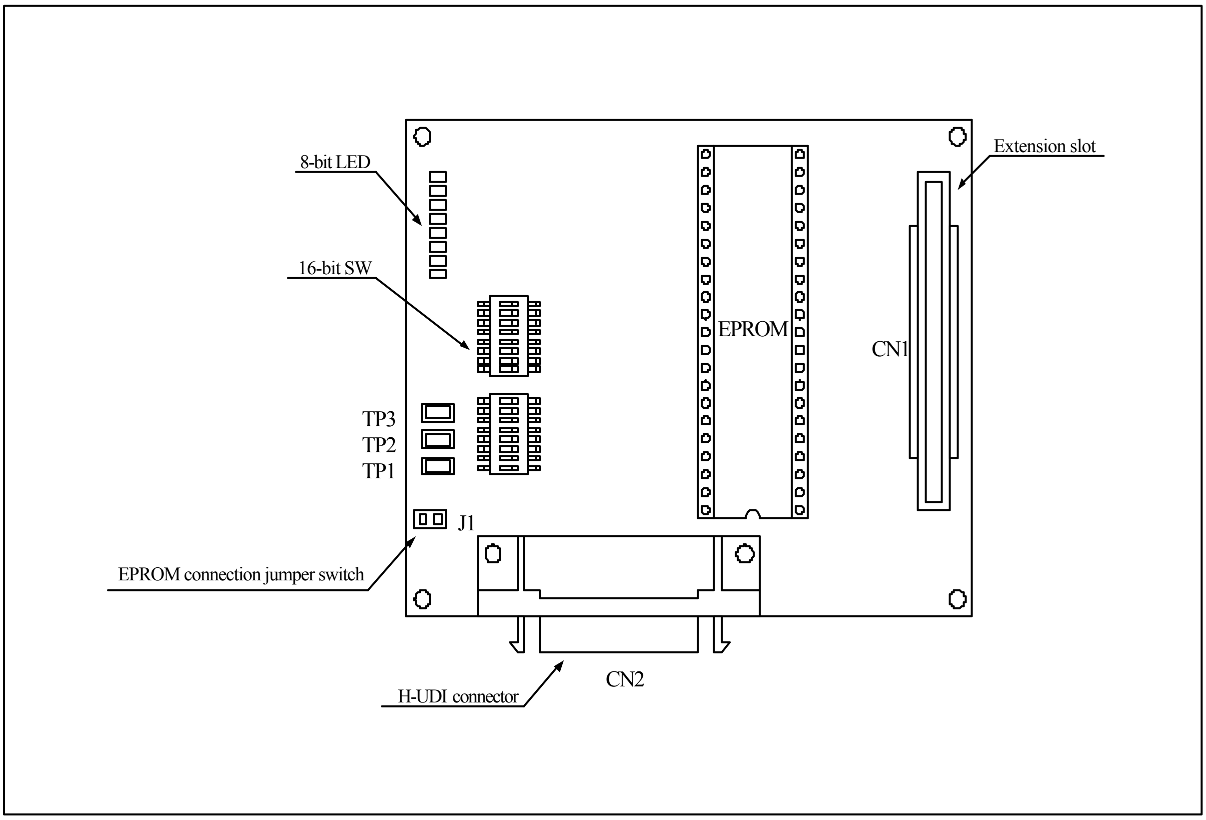


Figure 1.6 Debug Board - External View

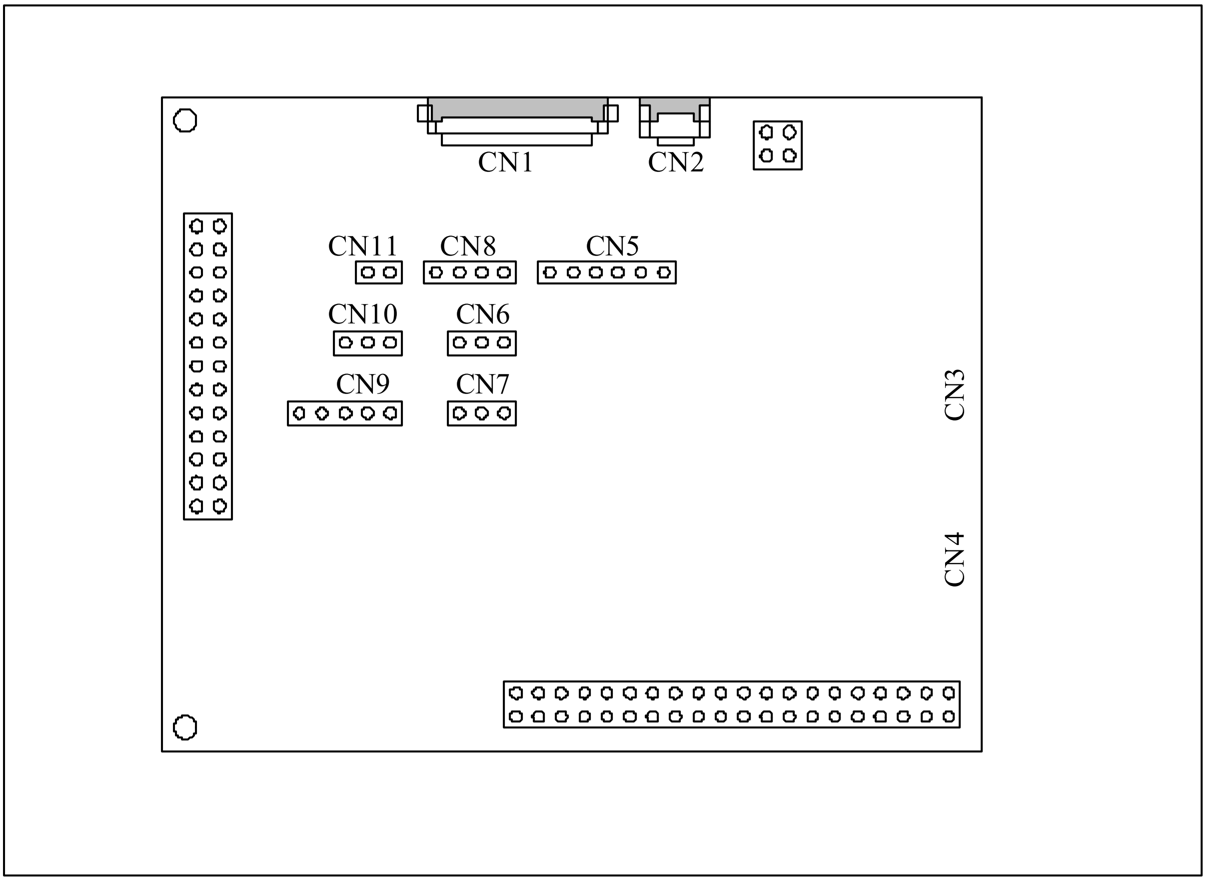


Figure 1.7 I/O Board - External View

1.4 T-Engine Specifications

Table 1-1 summarizes the T-Engine function specifications and Table 1-2 the power supply, dimensions, and environmental specifications.

Table 1-1 T-Engine Function Specifications

Item	Specifications	Target device
CPU	SH7760 Model name: HD6417760BP200D (RENESAS Technology) Input clock: 16.6667MHz Operating clock (Internal): 200MHz (x 12) (External): 66MHz (x 4) Package: 256-pin BGA	
Flash memory	Capacity: 8MB MBM29DL640E90TN (Fujitsu) x 1	
SDRAM	Capacity: 64MB EDS2516APTA-75 (ELPIDA) x 2	
PC Card I/F	One slot Controller: MR-SHPC-01 V2T (Marubun) Package: 144pin TQFP	
Serial I/F	2ch Controller: ST16C2550CQ48 (EXAR) Package: 48pin TQFP	ChA: H8/3048F-ONE I/F ChB: Monitor for debugging
Sound	Model name: UDA1342TS (Philips) Package: 28pin SSOP Earphone/microphone: 1ch Headphone output: 1ch - Microphone input Impedance: 2.2KΩ Sensitivity: -51dB/Pa - Headphone output Impedance: 32Ω	The SH7760 on-chip SSI is used to transmit data. The SH7760 on-chip IIC is used to select the mode.
USB Host	1ch Controller: SH7760 on-chip USB Host	
TFT color LCD module	NL2432DR22-02B (NEC) Display color: 262,144 colors Display area: 240(H) x 320(V) Controller:SH7760 on-chip LCDC	
Power supply controller	H8/3048F-ONE Model name: HD64F3048BVTE25 (Renesas Technology) Operating frequency: 7.3728MHz Package: 100-pin TQFP	The control SH7760 working for power supply control, RTC, or tablet interface infrared remote control must be interfaced via the serial chA.
RTC	Model name: RV5C348B (RICOH) Package: 10pin SSOP-G	Via the H8/3048F-ONE
Touch panel I/F	Model name: ADS7843 (TI) Package: 16pin SSOP	Via the H8/3048F-ONE (To be mounted on the LCD board)
Serial EEPROM	Capacity: 512 bytes Model name: S-29391AFJA (SII)	Via the H8/3048F-ONE
Infrared remote control	Transmission Model name: GL100MN0MP (SHARP) Transmission carrier: 38KHz Reception Model name: GP1UC101 (SHARP) Transmission carrier: 38KHz	Via theH8/3048F-ONE

Table 1.2 Power supply, Dimensions, and Environmental Specifications of the T-Engine Board

Item	Specifications
Environment	Operating conditions - Temperature: 10-35ºC - Humidity: 30 to 85% RH (no dew condensation occurs) Ambient gas: no corrosive gas
Operating voltage	DC 5.6VDC
Dissipation current	600mA
Dimensions	CPU board: 120mm x 75mm LCD board: 120mm x 75mm Debug board: 101mm x 75mm I/O board: 101mm x 75mm

Table 1.3 Permissible Current Supplied Externally by T-Engine Supply Voltage

Supply voltage	Permissible current	Locations subject to current supply
5V	250mA	• PCMCIA card power supply • USB bus power • Extension slot
3.3V	250mA	• PCMCIA card power supply • Extension slot

⚠ CAUTION

- Table 1.2 shows the maximum dissipation current of T-Engine (comprising only the CPU board, LCD board, debug board, and I/O board) without external devices.
- Table 1.3 shows the sum of permissible current in all the powered devices on T-Engine. Accordingly, when a current of 100mA is used for the PCMCIA card supply voltage (5V), the currents of the USB bus power or extension slot is 150mA (250mA to 100mA). This is true for the supply voltage 3.3V.
- When the PCMCIA card, etc. is powered from the internal power supply of T-Engine, the current must not exceed the permissible current of each power supply shown in Table 1.3. Otherwise, there is a risk of electric shock, heat, or fire.

2. Installation

2.1 Host System Connection

To use T-monitor, connect the serial interface connector (CN1) of the T-Engine board with an RS-232C interface cable (accessory). Figure 2.1 shows the host system connection method. Figure 2.2 shows the pins of the serial interface connector. Table 2.1 shows the signals of the serial interface connector.

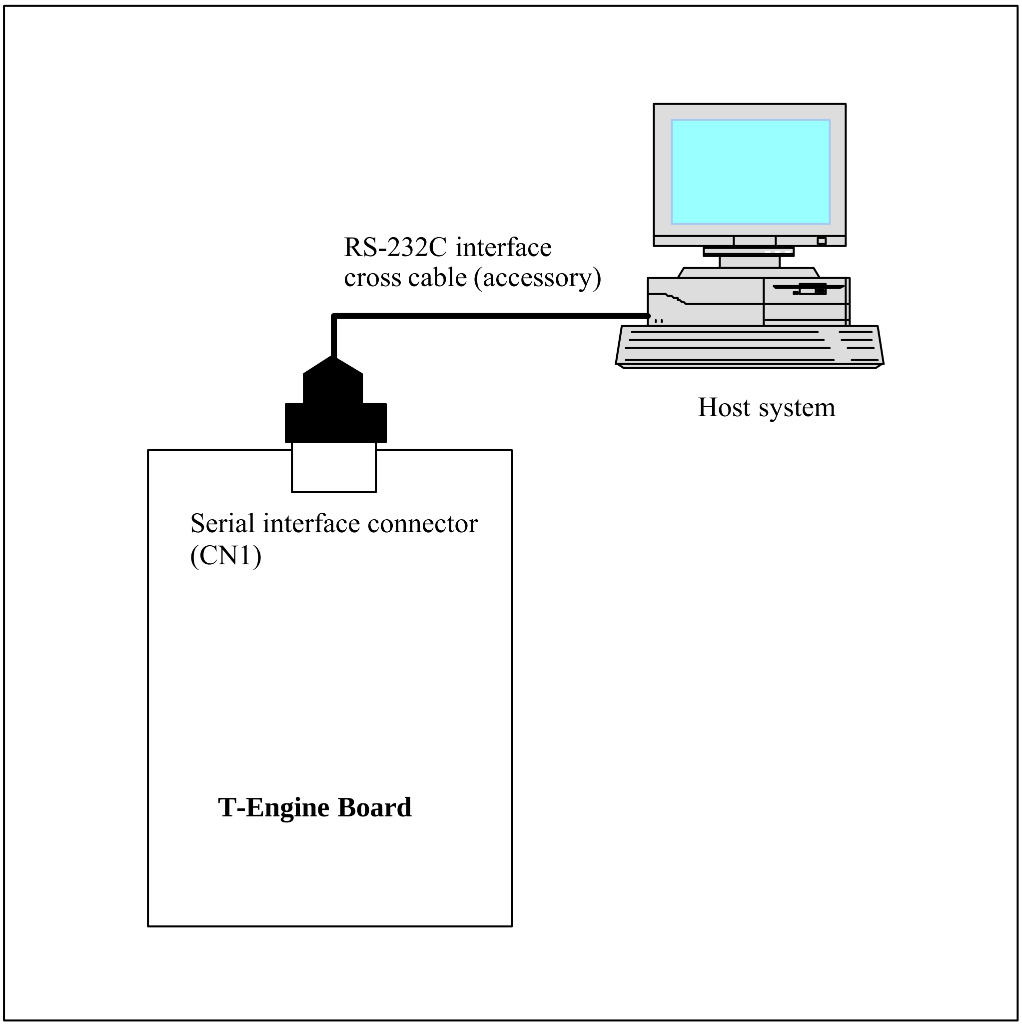


Figure 2.1 Host System Connection

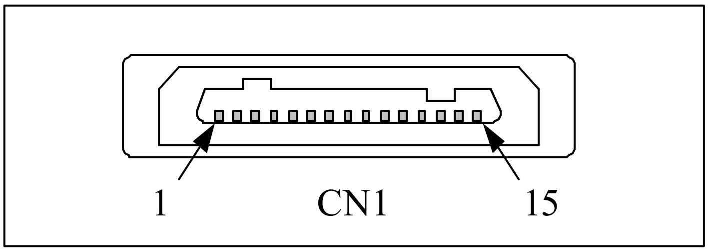


Figure 2.2 Serial Interface Connector Pins

Table 2.1 Serial Interface Connector Signals

Pin No.	Signal name	I/O	Remarks
1	GND	-	
2	TxD	Output	TXB(UART)
3	RxD	I	RXB(UART)
4	GND	-	
5	RTS	O	RTSB(UART)
6	CTS	I	CTSB(UART)
7	GND	-	
8	Reserved	-	ISP TCK(*)
9	Reserved	-	GND(*)
10	Reserved	-	ISP TMS(*)
11	Reserved	-	ISP Plug(*)
12	Reserved	-	ISP BScan(*)
13	Reserved	-	ISP TDI(*)
14	Reserved	-	ISP TDO(*)
15	Reserved	-	Vcc(3.3V) (*)

*: These pins are used only to test the board when it is shipped from the factory.

Don't use these pins for any other purpose.

2.2 AC Adapter Connection

Figure 2.3 shows an AC adapter connection method. As shown in Figure 2.3, connect the plug to the AC adapter connector of the T-Engine board (1), then connect the adapter cord to the receptacle (2).

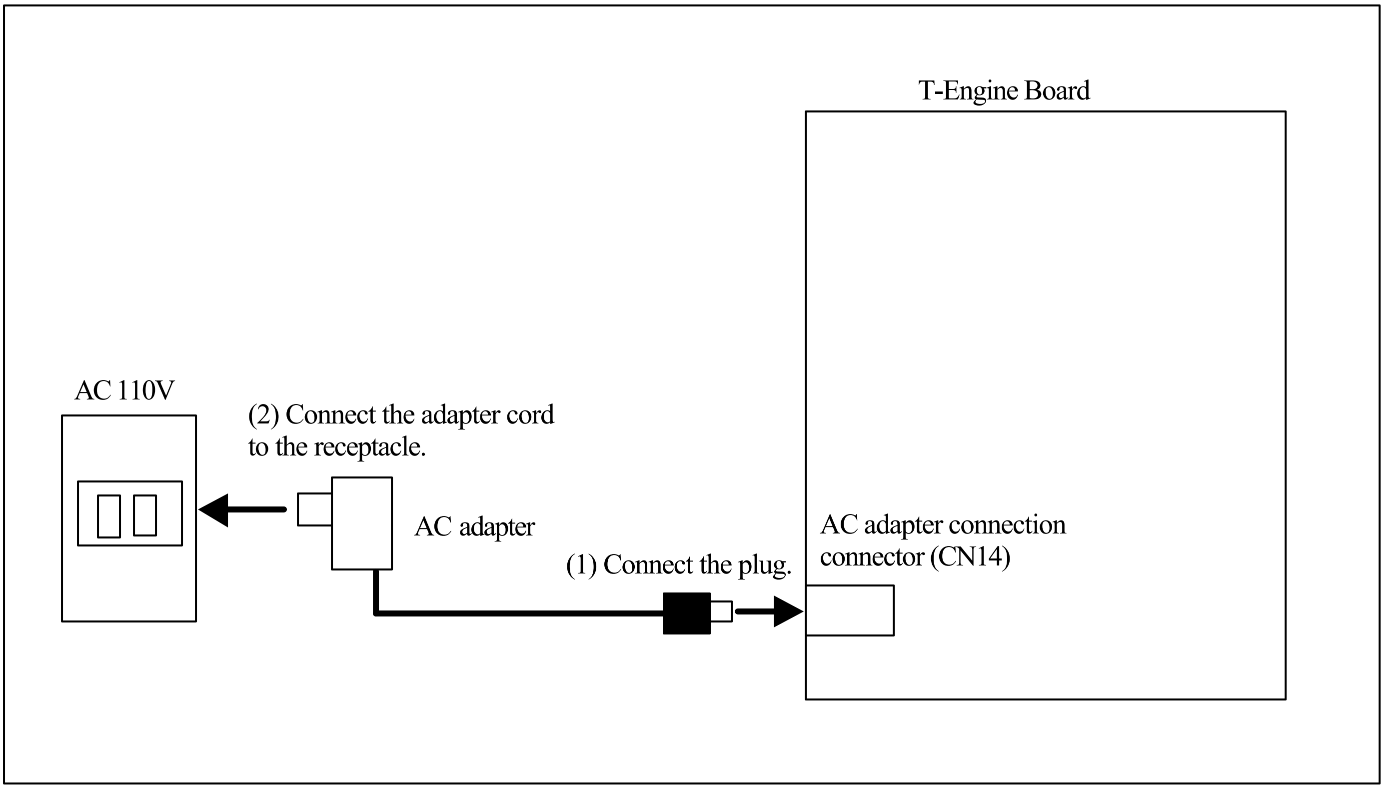


Figure 2.3 AC Adapter Connection Cord

⚠ CAUTION

- Don't put heavy things on the AC adapter cord. To avoid the risk of electric leakage, fire, or electric shock, don't damage or modify the AC adapter cord.
- To avoid the risk of electric shock, don't unplug the AC adapter cord with wet hands. To avoid the risk of cord damage, electric shock, or fire, don't pull on the AC adapter cord; rather, grasp and pull the plug to disconnect the AC adapter cord.
- When connecting the AC adapter to the receptacle, check the polarity and connection beforehand to avoid the risk of electric shock, fire, or fault.

2.3 Turning ON or OFF the T-Engine Board

To turn the T-Engine board ON or OFF, press the power-on switch (SW1) on the CPU board. To turn ON the T-Engine board, press and hold the switch for 0.5 seconds or more. To turn it OFF, press and hold this switch for 2 seconds or more while the T-Engine board is powered.

2.4 Using the Debug Board

2.4.1 Debug Board Function

When the debug board has been connected to the T-Engine, the following functions can be implemented:

(1) Run the program stored in the EPROM on the debug board to refresh the flash memory on the T-Engine board. The H8/3048F-One firmware can be refreshed. For details on flash memory refresh, refer to 10. "Flash Memory Refresh."

(2) The 8-bit LEDs on the debug board can be turned on or off from the SH7760. The software execution state can be monitored by controlling the ON/OFF state of these LEDs.

(3) The 16-bit SWs on the debug board can be read from the SH7760. Various operating conditions can be controlled through these SWs.

(4) The H-UDI debugger (to be connected to the H-UDI and AUD pins of the SH7760) can be used.

2.4.2 Debug Board Connection

Figure 2.4 shows a debug board connection method. Connect the debug board to the extension slot (CN2) on the T-Engine board.

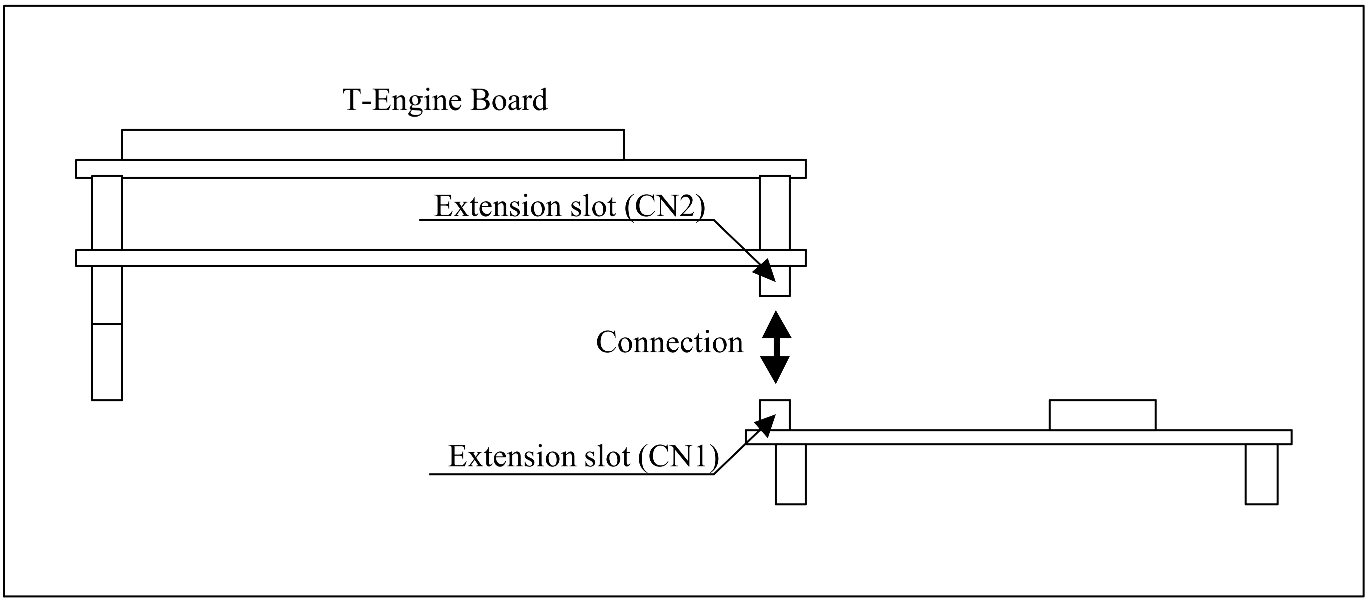


Figure 2.4 Debug Board Connection

CAUTION

Turn off the T-Engine before connecting the debug board or detaching the EPROM. When reattaching the EPROM, check the connecting direction as shown in Figure 2.5.

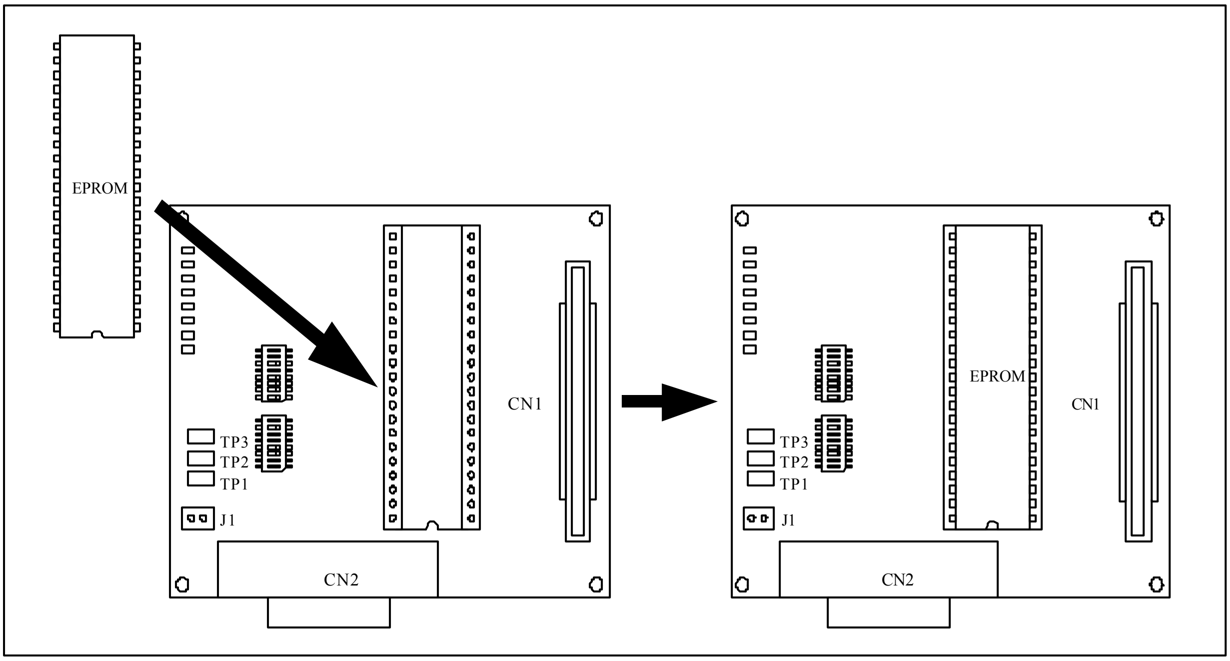
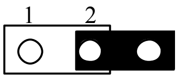
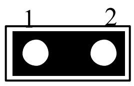


Figure 2.5 EPROM Connection

2.4.3 Debug Board Jumper Switches

Table 2.2 describes a method for setting the EPROM selection jumper switch (J1) on the debugger board. For details of a memory map during debug board connection, refer to 4. "Memory Map."

Table 2.2 Setting the EPROM Selection Jumper Switch (J1)

Jumper switch	Setting	Description
J1	 Pins 1 and 2 must be open	Debug board resources are assigned to area 0 on the SH7760 board as shown below. (Factory setting) - The flash memory on the T-Engine board is assigned to an address range from h'00000000 to h'007FFFFF. - The EPROM mounted on the debug board is assigned to an address range from h'01000000 to h'011FFFFF. - The 8-bit LEDs mounted on the debug board are assigned to an address range from h'014000000 to h'017FFFFF. - The 16-bit SWs mounted on the debug board are assigned to an address range from h'01800000 to h'01BFFFFF.
	 Pins 1 and 2 must be short-circuited.	Debug board resources are assigned to area 0 on the SH7760 board as shown below. - The EPROM mounted on the debug board is assigned to an address range from h'00000000 to h'001FFFFF. - The 8-bit LEDs mounted on the debug board are assigned to an address range from h'00400000 to h'007FFFFF. - The 16-bit SWs mounted on the debug board are assigned to an address range from h'00800000 to h'00BFFFFF. - The flash memory on the T-Engine board is assigned to an address range from h'01000000 to h'017FFFFF.

2.4.4 8-bit LEDs on the Debug Board

The low-order 8 bits (D7 to D0) of the SH7760 data bus are connected to the 8-bit LEDs placed on the debug board. The 8-bit LEDs can be turned on or off by writing data to an area assigned for the LEDs through D7 to D0. When a value of 1 is written to a bit, the corresponding LED is turned off. When a value of 0 is written to the bit, it is turned on.

2.4.5 16-bit SWs on the Debug Board

The 16 bits (D15 to D0) of the SH7760 are connected to the 16-bit SWs placed on the debug board. The 16-bit SWs can be turned on or off by reading data from an area assigned for the SWs through D15 to D0. When a value of 1 is read from a bit, the corresponding SW is turned off. When a value of 0 is read from the bit, the corresponding SW is turned on.

2.4.6 H-UDI Debugger Connection

The debug board allows the H-UDI debugger to be connected to the pin 36 (CN2) of the H-UDI (Hitachi-User Debug Interface) connector. Connect the H-UDI and AUD pins of the SH7760 board to the H-UDI connector. Figure 2. 6 shows a method for connecting the H-UDI debugger. Connect an H-UDI debugger cable to the H-UDI connector (CN2) of the debug board. Note that the following H-UDI debugger can be connected to T-Engine. For details on the H-UDI debugger connection/setup procedure, refer to the pertinent manual of the product.

- Renesas Technology Corporation
  E10A-USB Emulator Model name: HS0005KCU02H (AUD)
- Hitachi ULSI Systems Co., Ltd.
  MY-ICE EZ emulator

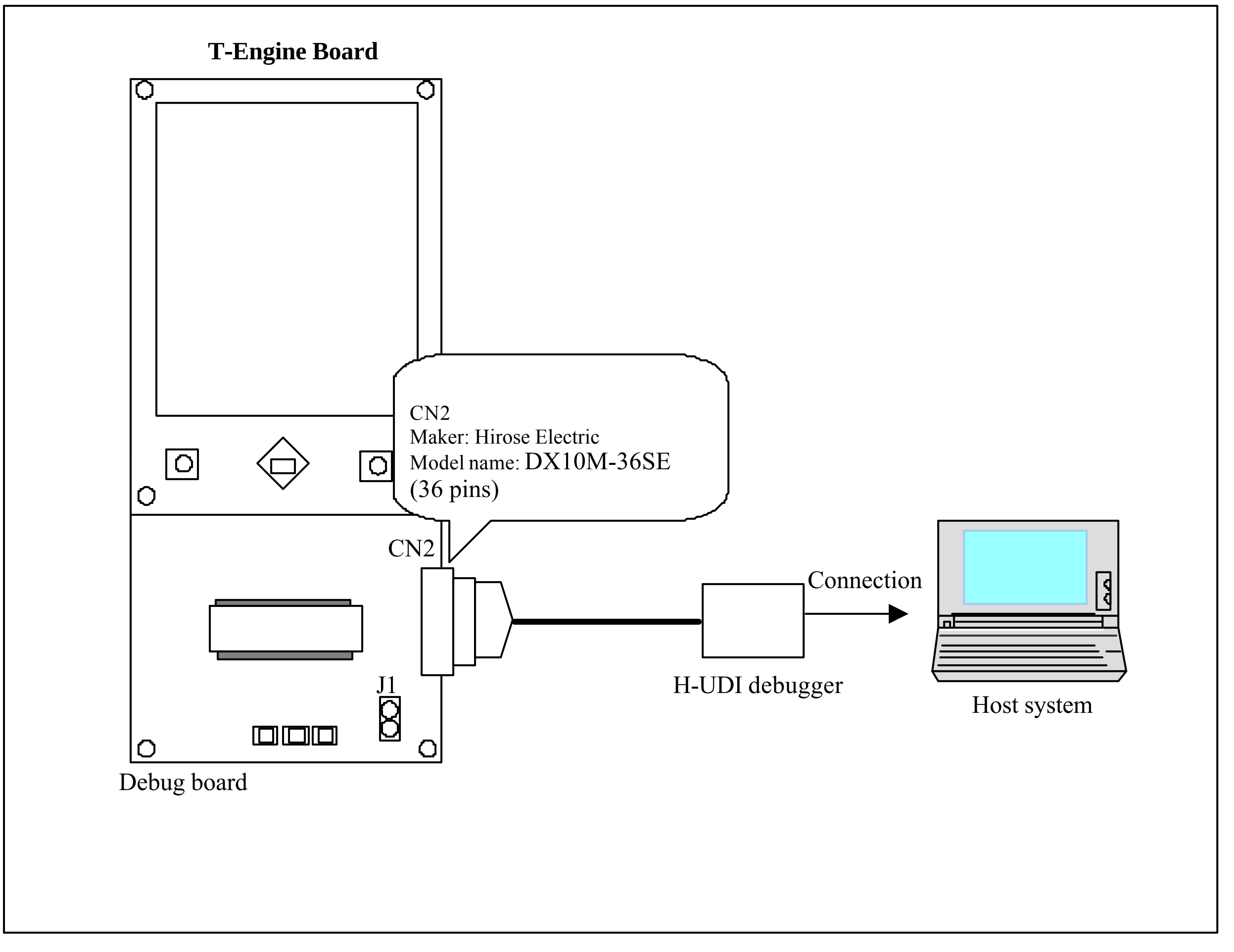


Figure 2.6 H-UDI Debugger Connection

⚠ CAUTION

T-Engine permits the connection of only the H-UDI debugger that uses the AUD and H-UDI pins of the SH7760 board.

3. Switches

3.1 CPU Board Switches

Figure 3.1 shows the location of the switches (SW1 to SW5) on the CPU board. In addition, this section gives a brief description of each switch in (1) to (5).

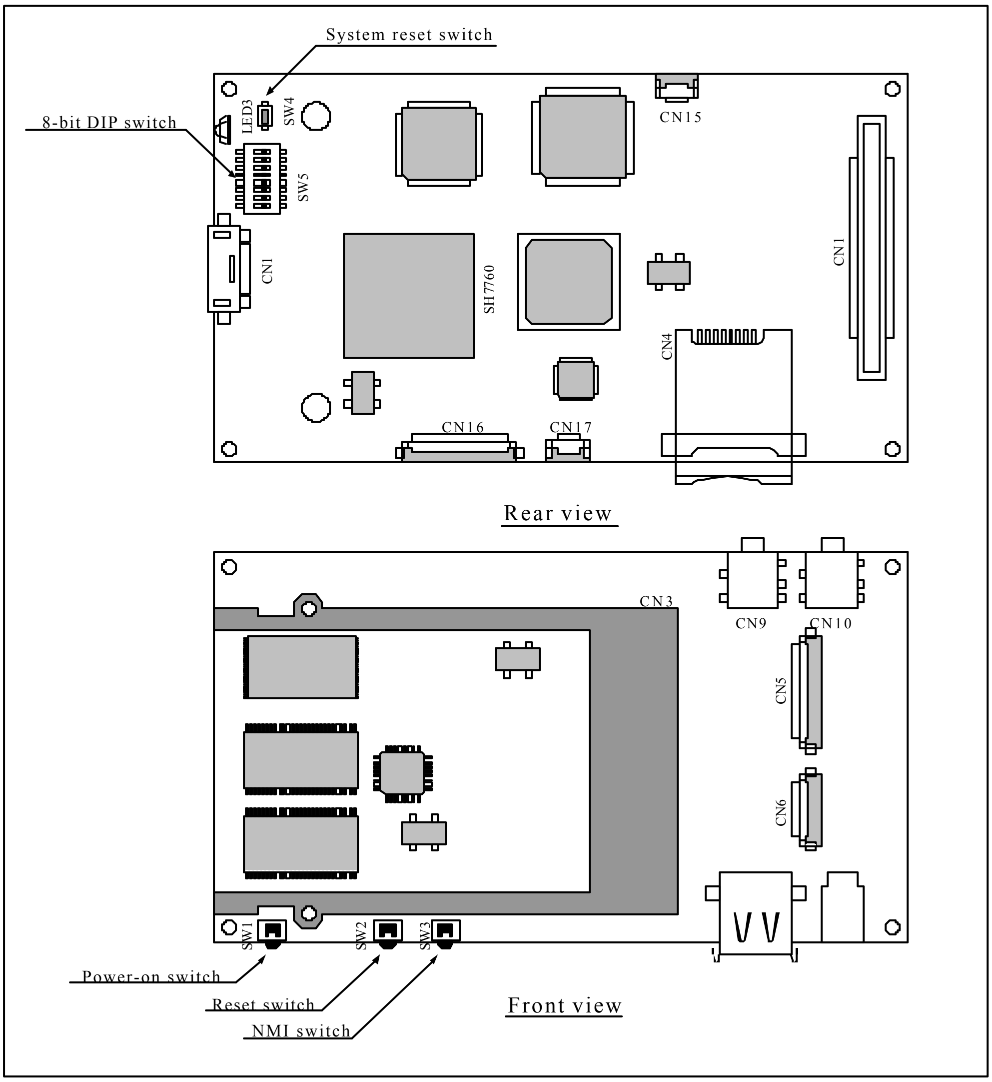


Figure 3.1 CPU Board Switches (SW1 to SW5)

(1) Power on Switch (SW1)

This switch turns on or off T-Engine. To turn on T-Engine, press and hold down this switch for 0.5 seconds or more. To turn it off, press and hold down this switch for 2 seconds or more when T-Engine is being powered.

(2) Reset Switch (SW2)

This switch resets T-Engine. To reset devices other than the H8/3048-ONE, press this switch. To reset and restart T-Engine, release this switch. In this case, the values of H8/3048-ONE internal registers are not initialized. Among the control registers, the values of those that can be accessed by SH7760 are initialized but the others are not (i.e., their values are retained). For more details, refer to 6.13 “Initial Values of the Power Supply Controller Register.”

(3) NMI Switch (SW3)

This switch controls the SH7760 NMI pin. Press this switch and the SH7760 NMI pin will go "Low." Release this switch, and the NMI pin will go "High."

(4) 8-bit DIP Switch (SW5)

Figure 3.2 shows the setting of an 8-bit DIP switch. This DIP switch is connected to pins ID0 to ID5 and to MD5 of the SH7760. Be sure to turn off the power-on switch before setting the DIP switch.

(a) Switches SW5-1 to SW5-6 are connected to pins ID0 to ID5 (input pins).

ON: The input pin goes "Low."

OFF: The input pin goes "High." (Factory setting)

(b) The SW5-7 switch is used to set the power-on condition of T-Engine.

ON: T-Engine is powered when power supply takes place through the AC adapter.

OFF: T-Engine is powered when the power-on switch is pressed. (Factory setting)

(c) The SW5-8 switch is connected to SH7760's pin MD5. The SW5-8 switch is used to set the type of endian for SH7760 operation.

ON: The MD5 pin goes "Low" to set the big endian for SH7760 operation.

OFF: The MD5 pin goes "High" to set the little endian for SH7760 operation. (Factory setting)

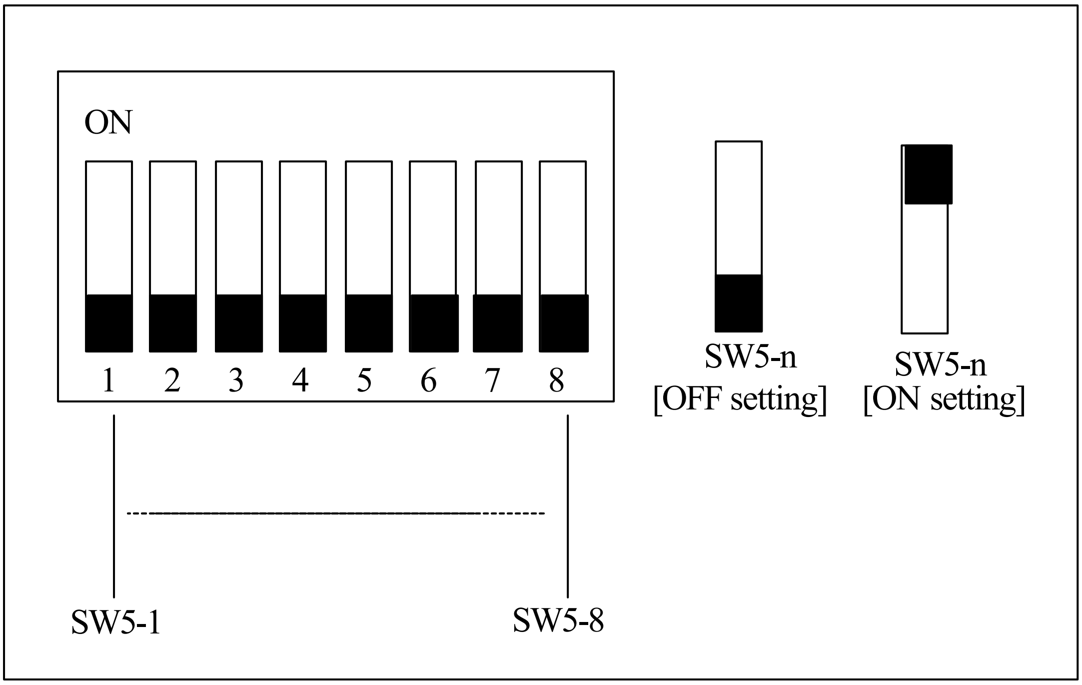


Figure 3.2 Setting the 8-bit DIP Switch

(5) System Reset Switch (SW4)

This switch resets the T-Engine hardware. All T-Engine devices are reset so long as this switch is pressed and held down. When this switch is released, T-Engine is turned off. When the power-on switch is pressed,

T-Engine is turned on and started. In addition, if this switch is released while SW5-7 is ON, T-Engine is also turned on.

3.2 LCD Board Switch

The states of the cursor switch (SW1) and push-button switches (SW2 and SW3) are signaled to the SH7760 through the power supply controller. For details, refer to 6. "Power Supply Controller."

4. Memory Map

4.1 Memory Map for the T-Engine Board

Table 4.1 shows an SH7760 memory map for the T-Engine board without expansion board.

Table 4.1 SH7760 Memory Map for T-Engine without Expansion Board

Area No.	Bus width	Space	Space name	Device	Remarks
Area 0	16 bits	h'00000000 ~ h'00FFFFFF	Flash memory area	8MB MBM29DL640E-90TN (Fujitsu) x 1	
		h'00100000 ~ h'03FFFFFF	-	Unused area	
Area 1	16 bits	h'04000000 ~ h'07FFFFFF	Board control register area	16B Board control register	
Area 2	8/16/32 bits	h'08000000 ~ h'0BFFFFFF	Extension area (CS2)	64MB Extension slot (CS2 area)	Extension slot CS2# asserted
Area 3	32 bits	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-75 (ELPIDA) x 2	
Area 4	8/16/32 bits	h'10000000 ~ h'13FFFFFF	Extension area (CS4)	64MB Extension slot (CS4 area)	Extension slot CS4# asserted
Area 5	8/16/32 bits	h'14000000 ~ h'17FFFFFF	Extension area (CS5)	64MB Extension slot (CS5 area)	Extension slot CS5# asserted
Area 6	16 bits	h'18000000 ~ h'19FFFFFF	PCMCIA area	Card controller Model name: MR-SHPC-01 V2T (Marubun) This device is simply called SH-PCIC.	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model name: ST16C2550CQ48 (EXAR) This device is simply called UART.	This device is used for interface with H8/3048F-ONE.
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	This device is used as an interface with the host.
		h'1B000000 ~ h'1BFFFFFF	ID register area	-	The DIP switch settings are read.
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

4.2 Memory Map during Debug Board Connection

Table 4.2 shows a memory map for the SH7760 when the debug board is connected to the T-Engine board and the jumper switch (J1) on the debug board is open. Table 4.3 also shows a memory map for the SH7760 when the debug board is connected to the T-Engine board and the jumper switch (J1) on the debug board is short-circuited.

Table 4.2 Memory Map during Debug Board Connection (J1: Open)

Area No.	Bus width	Space	Space name	Device	Remarks
Area 0	16 bits	h'00000000 ~ h'00FFFFFF	Flash memory area	8MB MBM29DL640E-90TN (Fujitsu) x 1	
		h'01000000 ~ h'013FFFFF	EPROM area	256kB M27C800-100F1 (STMicro) x 1	Resources on the debug board
		h'01400000 ~ h'017FFFFF	Debug LED area	1B 8-bit debug LED	
		h'01800000 ~ h'01BFFFFF	Switch area	2B 8-bit switch x 2	
		h'01C00000 ~ h'01FFFFFF		Unused area	
		h'02000000 ~ h'03FFFFFF	-	Unused area	
Area 1	16 bits	h'04000000 ~ h'07FFFFFF	Board control register area	16B Board control register	
Area 2	8/16/32 bits	h'08000000 ~ h'0BFFFFFF	Extension area (CS2)	64MB Extension slot (CS2 area)	Extension slot CS2# asserted
Area 3	32 bits	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-75 (ELPIDA) x 2	
Area 4	8/16/32 bits	h'10000000 ~ h'13FFFFFF	Extension area (CS4)	64MB Extension slot (CS4 area)	Extension slot CS4# asserted
Area 5	8/16/32 bits	h'14000000 ~ h'17FFFFFF	Extension area (CS5)	64MB Extension slot (CS5 area)	Extension slot CS5# asserted
Area 6	16 bits	h'18000000 ~ h'19FFFFFF	PCMCIA area	Card controller Model name: MR-SHPC-01 V2T(Marubun) This device is simply called SH-PCIC.	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model name: ST16C2550CQ48(EXAR) This device is simply called UART.	This device is used for interface with H8/3048F-ONE.
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	This device is used as an interface with the host.
		h'1B000000 ~ h'1BFFFFFF	ID register area		The DIP switch settings are read.
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

Table 4.3 Memory Map during Debug Board Connection (J1: short-circuited)

Area No.	Bus width	Space	Space name	Device	Remarks
Area 0	16 bits	h'00000000 ~ h'003FFFFF	EPROM area	256kB M27C800-100F1 (ST Micro) x 1	Resources on the debug board
		h'00400000 ~ h'007FFFFF	Debug LED area	1B 8-bit debug LED	
		h'00800000 ~ h'00BFFFFF	Switch area	2B 8-bit switch x 2	
		h'00C00000 ~ h'00FFFFFF		Unused area	
		h'01000000 ~ h'01FFFFFF	Flash memory area	8MB MBM29DL640E-90TN (Fujitsu) x 1	
		h'02000000 ~ h'03FFFFFF	-	Unused area	
Area 1	16 bits	h'04000000 ~ h'07FFFFFF	Board control register area	16B Board control register	
Area 2	8/16/32 bits	h'08000000 ~ h'0BFFFFFF	Extension area (CS2)	64MB Extension slot (CS2 area)	Extension slot CS2# asserted
Area 3	32 bits	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-75 (ELPIDA) x 2	
Area 4	8/16/32 bits	h'10000000 ~ h'13FFFFFF	Extension area (CS4)	64MB Extension slot (CS4 area)	Extension slot CS4# asserted
Area 5	8/16/32 bits	h'14000000 ~ h'17FFFFFF	Extension area (CS5)	64MB Extension slot (CS5 area)	Extension slot CS5# asserted
Area 6	16 bits	h'18000000 ~ h'19FFFFFF	PCMCIA area	Card controller Model name: MR-SHPC-01 V2T(Marubun) This device is simply called SH-PCIC.	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model name: ST16C2550CQ48(EXAR) This device is simply called UART.	This device is used for interface with H8/3048F-ONE.
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	This device is used as an interface with the host.
		h'1B000000 ~ h'1BFFFFFF	ID register area		The DIP switch settings are read.
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

5. Functional Blocks

5.1 PCMCIA

5.1.1 Block Description

Figure 5.1 shows the PCMCIA control block. As shown in Figure 5.1, the PCMCIA control block contains a controller (MR-SHPC-01 V2 from Marubun Corporation), a 68-pin PC card interface connector (CN3) and a power supply controller IC (TPS2211DB from TI). This controller interfaces with the card(s) conforming to the PC Card Standard 97 and has the following features:

- Internal memory windows (2 windows) and I/O window (one window)
- Card access timing adjustment function
- One-step read/write buffer
- Endian internal control circuit
- Support for 5.0V/3.3V cards
- External buffer not required
- Internal interrupt steering function
- Power-down function
- Internal suspend function

There are four kinds of controller interrupts (SIRQ3 to SIRQ0). hputs to the H7760 are made by the IRL codes. For details, refer to Marubun's MR-SHPC-01 V2 Manual.

Marubun Homepage: http://www.marubun.co.jp

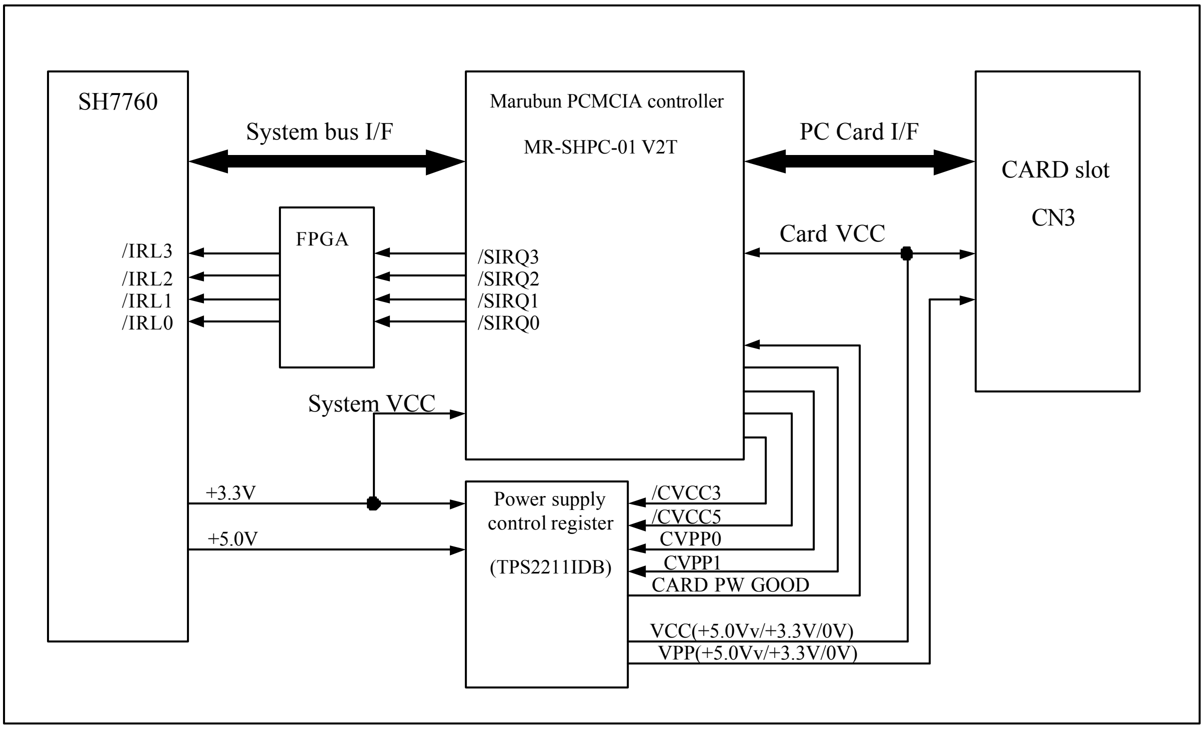


Figure 5.1 PCMCIA Control Block

5.1.2 Connector Pins

Table 5.1 summarizes the pins of a 68-pin PC card interface connector (CN3).

Table 5.1(1) PC Card Interface Connector Signal Pins

Pin	Memory card			I/O card		
	Signal name	I/O	Function	Signal name	I/O	Function
1	GND	-	Ground	GND	-	Ground
2	D3	I/O	Data bit 3	D3	I/O	Data bit 3
3	D4	I/O	Data bit 4	D4	I/O	Data bit 4
4	D5	I/O	Data bit 5	D5	I/O	Data bit 5
5	D6	I/O	Data bit 6	D6	I/O	Data bit 6
6	D7	I/O	Data bit 7	D7	I/O	Data bit 7
7	CE1#	I	Card enable	CE1#	I	Card enable
8	A10	I	Address bit 10	A10	I	Address bit 10
9	OE#	I	Output enable	OE#	I	Output enable
10	A11	I	Address bit 11	A11	I	Address b it 11
11	A9	I	Address bit 9	A9	I	Address bit 9
12	A8	I	Address bit 8	A8	I	Address bit 8
13	A13	I	Address bit 13	A13	I	Address bit 13
14	A14	I	Address bit 14	A14	I	Address bit 14
15	WE#	I	Write enable	WE#	I	Write enable
16	READY	O	Ready	IREQ#	O	Interrupt request
17	Vcc	-	Supply voltage	Vcc	-	Supply voltage
18	VPP1	-	Programmed supply voltage	VPP1	-	Programmed supply voltage
19	A16	I	Address bit 16	A16	I	Address bit 16
20	A15	I	Address bit 15	A15	I	Address bit 15
21	A12	I	Address bit 12	A12	I	Address bit 12
22	A7	I	Address bit 7	A7	I	Address bit 7
23	A6	I	Address bit 6	A6	I	Address bit 6
24	A5	I	Address bit 5	A5	I	Address bit 5
25	A4	I	Address bit 4	A4	I	Address bit 4
26	A3	I	Address bit 3	A3	I	Address bit 3
27	A2	I	Address bit 2	A2	I	Address bit 2
28	A1	I	Address bit 1	A1	I	Address bit 1
29	A0	I	Address bit 0	A0	I	Address bit 0
30	D0	I/O	Data bit 0	D0	I/O	Data bit 0
31	D1	I/O	Data bit 1	D1	I/O	Data bit 1
32	D2	I/O	Data bit 2	D2	I/O	Data bit 2
33	WP	O	Write Protect	IOIS16#	O	16bit I/O port
34	GND	-	Ground	GND	-	Ground

Table 5.1(2) PC Card Interface Connector Signal Pins

Pin	Memory card			I/O card		
	Signal name	I/O	Function	Signal name	I/O	Function
35	GND	-	Ground	GND	-	Ground
36	CD1#	O	Card detection	CD1#	O	Card detection
37	D11	I/O	Data bit 11	D11	I/O	Data bit 11
38	D12	I/O	Data bit 12	D12	I/O	Data bit 12
39	D13	I/O	Data bit 13	D13	I/O	Data bit 13
40	D14	I/O	Data bit 14	D14	I/O	Data bit 14
41	D15	I/O	Data bit 15	D15	I/O	Data bit 15
42	CE2#	I	Card enable	CE2#	I	Card enable
43	VS1#	O	Voltage sense	VS1#	O	Voltage sense
44	RFU	-	Reserved	IORD#	I	I/O read
45	RFU	-	Reserved	IOWR#	I	I/O write
46	A17	I	Address bit 17	A17	I	Address bit 17
47	A18	I	Address bit 18	A18	I	Address bit 18
48	A19	I	Address bit 19	A19	I	Address bit 19
49	A20	I	Address bit 20	A20	I	Address bit 20
50	A21	I	Address bit 21	A21	I	Address bit 21
51	Vcc	-	Supply voltage	Vcc	-	Supply voltage
52	VPP2	-	Programmed supply voltage	VPP2	-	Programmed supply voltage
53	A22	I	Address bit 22	A22	I	Address bit 22
54	A23	I	Address bit 23	A23	I	Address bit 23
55	A24	I	Address bit 24	A24	I	Address bit 24
56	A25	I	Address bit 25	A25	I	Address bit 25
57	VS2#	O	Voltage sense	VS2#	O	Voltage sense
58	RESET	I	Card reset	RESET	I	Card reset
59	WAIT#	O	Bus cycle extension	WAIT#	O	Bus cycle extension
60	RFU	-	Reserved	INPACK#	O	I/O port response
61	REG#	I	Register selection	REG#	I	Register selection
62	BVD2	O	Battery voltage detection	SPKR#	O	Audio digital waveform
63	BVD1	O	Battery voltage detection	STSCHG#	O	Card status change
64	D8	I/O	Data bit 8	D8	I/O	Data bit 8
65	D9	I/O	Data bit 9	D9	I/O	Data bit 9
66	D10	I/O	Data bit 10	D10	I/O	Data bit 10
67	CD2#	O	Card detection	CD2#	O	Card detection
68	GND	-	Ground	GND	-	Ground

5.1.3 Register Map

Table 5.2 shows a map for the PCMCIP controller registers. Each of the controller registers must be accessed in words.

Table 5.2 PCMCIA Control Registers

Address	Initial value	Register name
H’B83FFFE4	H’0000	Mode register
H’B83FFFE6	H’000C	Option register
H’B83FFFE8	H’03BF	Card status register
H’B83FFFEA	H’0000	Interrupt factor register
H’B83FFFEC	H’0000	Interrupt control register
H’B83FFFEE	H’0000	Card voltage control register
H’B83FFFF0	H’07FC	Memory window 0 Control register 1
H’B83FFFF2	H’07FC	Memory window 1 Control register 1
H’B83FFFF4	H’07FC	I/O window Control register 1
H’B83FFFF6	H’0000	Memory window 0 Control register 2
H’B83FFFF8	H’0000	Memory window 1 Control register 2
H’B83FFFFA	H’0000	I/O window Control register 2
H’B83FFFFC	H’0000	Card control register
H’B83FFFFE	H’5333	Chip information register

5.2 USB Host

5.2.1 Block Description

Figure 5.2 shows the USB host control block. As shown in Figure 5.2, the SH7760 contains the internal USB host controller. This internal controller supports USB Versions 1.1openHCI has the following features:

- Compatibility with the OpenHCI Version 1.0a register set
- Conforms to the USB Version 1.1
- Provides a route hub function
- Supports the low speed (1.5Mbps) and full speed (12MB) modes
- Supports an overcurrent detection function
- Supports a maximum of 127 endpoints
- Capable of using the shared memory (8K) for transfer data and descriptors

For details, refer to the pertinent SH7760 Hardware Manual.

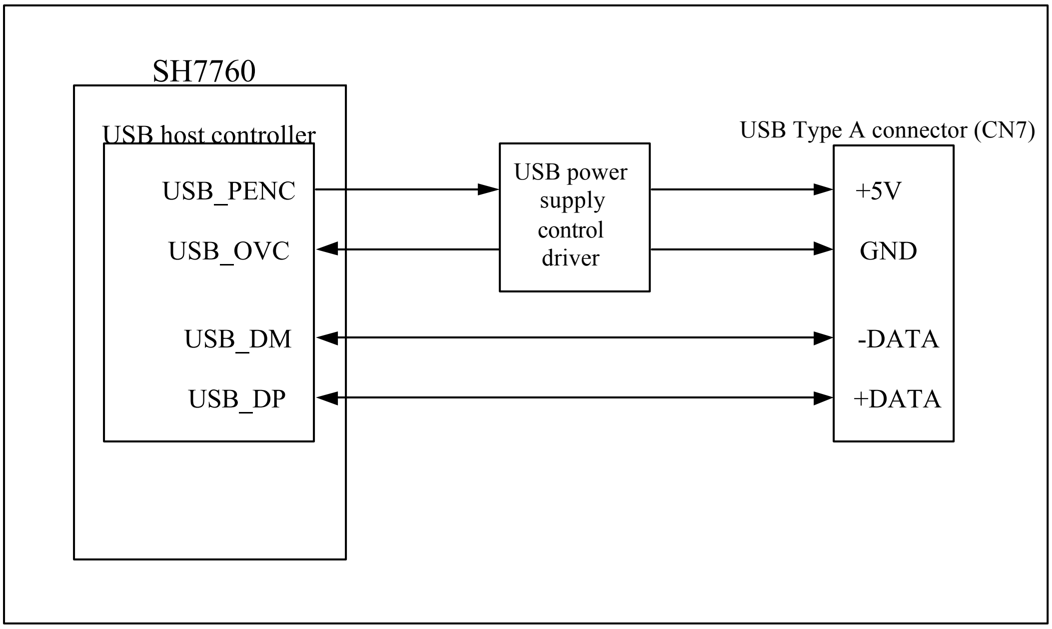
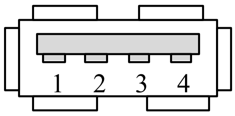


Figure 5.2 USB Host Control Block

5.2.2 Connector Pins

Figure 5.3 shows the pins of the USB host connector (CN7).



CN7 USB host connector (TypeA)
Model name: 20-5041-004-100-834
Maker: Kyocera Elco

Pin No	Signal name
1	VBUS
2	-DATA
3	+DATA
4	GND

Figure 5.3 USB Host Connector (CN7) Pins

5.2.3 Register Map

Table 5.3 shows a register map for the internal USB host controller of the SH7760.

Table5.3 USB Host Controller Register

Address	Initial value	Register name
H'FE340000	H'00000010	HcRevision register
H'FE340004	H'00000000	HcControl register
H'FE340008	H'00000000	HcCommandStatus register
H'FE34000C	H'00000000	HcInterruptStatus register
H'FE340010	H'00000000	HcInterruptEnable register
H'FE340014	H'00000000	HcInterruptDisable register
H'FE340018	H'00000000	HcHCCA register
H'FE34001C	H'00000000	HcPeriodCurrentED register
H'FE340020	H'00000000	HcControlHeadED register
H'FE340024	H'00000000	HcControlCurrentED register
H'FE340028	H'00000000	HcBulkHeadED register
H'FE34002C	H'00000000	HcBulkCurrentED register
H'FE340030	H'00000000	HcDonrHeadED register
H'FE340034	H'00002EDF	HcFmInterval register
H'FE340038	H'00000000	HcFrameRemaining register
H'FE34003C	H'00000000	HcFmNumber register
H'FE340040	H'00000000	HcPeriodicStart register
H'FE340044	H'00000628	HcLSThreshold register
H'FE340048	H'02001202	HcRhDescriptorA register
H'FE34004C	H'00000000	HcRhDescriptorB register
H'FE340050	H'00000000	HcRhStatus register
H'FE340054	H'00000100	HcRhPortStatus1 register
H'FE341000~ H'FE342FFF	-	Shared memory area

5.3 UART

5.3.1 Block Description

Figure 5.4 shows the UART control block. As shown in Figure 5.4, the UART control block contains the controller (ST16C2550 from EXAR), RS232C interface driver, and 15-pin connector (CN1). This controller uses the clock pulses (7.3728MHz) supplied from the power supply controller (H8/3048F-ONE) for operations, and determines a baud rate (transfer rate) using these pulses as reference.

This controller has been provided with a 2-channel UART device. Channel A is used to communicate with the power supply controller (H8/3048F-ONE). Because channel B is connected to a 15-pin RS-232C connector (CN1), it can be used as a debug interface if it is connected to a PC.

In addition, channel A (INTA) inputs the controller interrupts to the SH7760 IRL9 and channel B (INTB) inputs them to the SH7760 IRL11.

EXAR Homepage: http://www.exar.com

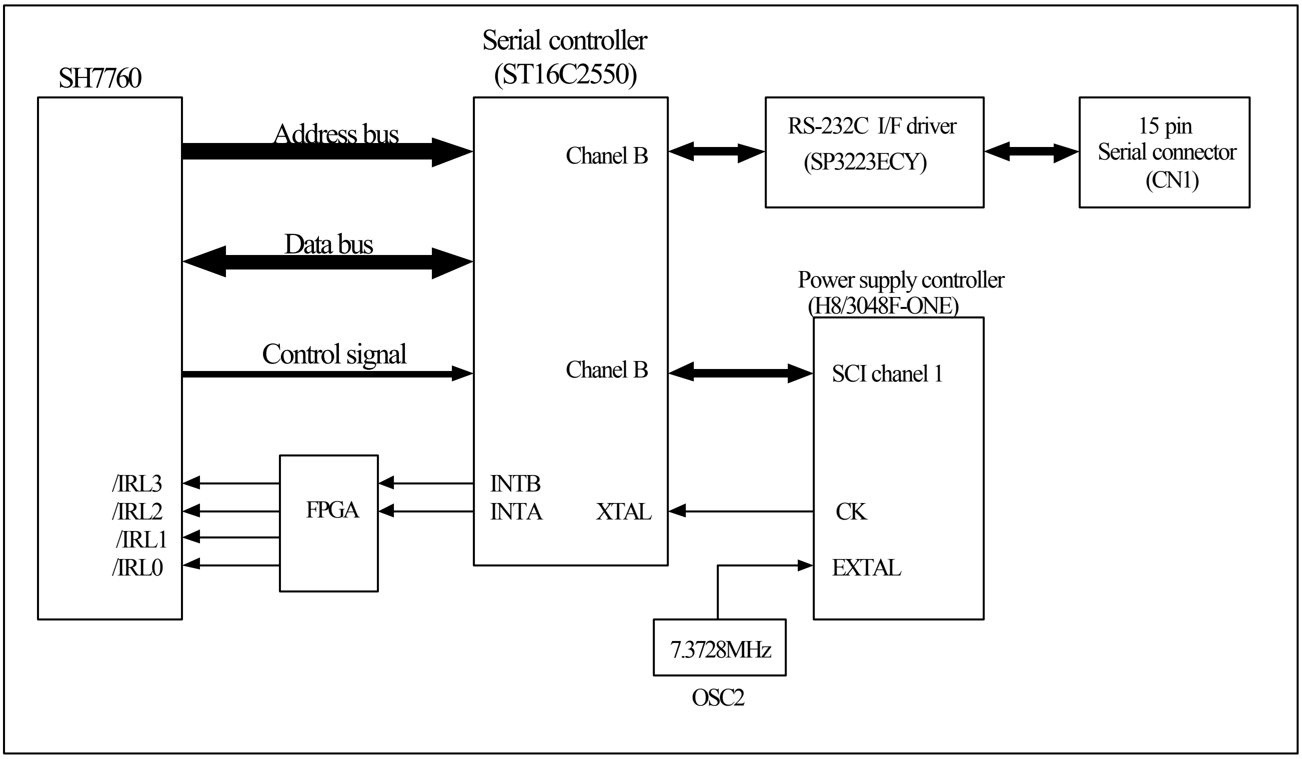
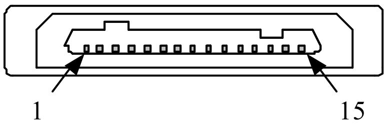


Figure 5.4 Serial Interface Block

5.3.2 Connector Pins

Figure 5.5 shows the pins of a 15-pin serial interface connector (CN1).



CN1: 15-pin serial connector
Model name: RMC-EA15MY-OM15-MC1
Maker: Honda Tsushin kogyo

Pin No	Signal name
1	GND
2	TxD
3	RxD
4	GND
5	RTS
6	CTS
7	GND
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 5.5 15-pin Serial Interface Connector Pins (CN1)

5.3.3 Register Map

Tables 5.4 and 5.5 show register maps for the serial interface controller registers. Each of the serial interface control registers must be accessed in words. If access takes place in words, data in the low order 8 bits (D7 to D0) will become effective.

Table 5.4 Serial Interface Controller Register Map (Channel A)

Address	Initial value	Register name (at read)	Register name (at write)	Remarks
H'BA000000	-	RHR (ReceiveHoldingRegister)	THR (TransferHoldingRegister)	LCR bit7=0
H'BA000000	-	DLL (LSB of Divisor Latch)	DLL (LSB of Divisor Latch)	LCR bit7=1
H'BA000002	H'00	IER (InterruptEnableRegister)	IER (InterruptEnableRegister)	LCR bit7=0
H'BA000002	-	DLM (MSB of Divisor Latch)	DLM (MSB of Divisor Latch)	LCR bit7=1
H'BA000004	H'01	ISR (InterruptStatusRegister)	FCR (FIFOControlRegister)	
H'BA000006	H'00	LCR (LineControlRegister)	LCR (LineControlRegister)	
H'BA000008	H'00	MCR (ModemControlRegister)	MCR (ModemControlRegister)	
H'BA00000A	H'60	LSR (LineStatusRegister)	N.A	
H'BA00000C	H'X0	MSR (ModemStatusRegister)	N.A	
H'BA00000E	H'FF	SPR (ScratchpadRegister)	SPR (ScratchpadRegister)	

Table 5.5 Serial Interface Controller Register Map (Channel B)

Address	Initial value	Register name (at read)	Register name (at write)	Remarks
H'BA800000	-	RHR (ReceiveHoldingRegister)	THR (TransferHoldingRegister)	LCR bit7=0
H'BA800000	-	DLL (LSB of Divisor Latch)	DLL (LSB of Divisor Latch)	LCR bit7=1
H'BA800002	H'00	IER (InterruptEnableRegister)	IER (InterruptEnableRegister)	LCR bit7=0
H'BA800002	-	DLM (MSB of Divisor Latch)	DLM (MSB of Divisor Latch)	LCR bit7=1
H'BA800004	H'01	ISR (InterruptStatusRegister)	FCR (FIFOControlRegister)	
H'BA800006	H'00	LCR (LineControlRegister)	LCR (LineControlRegister)	
H'BA800008	H'00	MCR (ModemControlRegister)	MCR (ModemControlRegister)	
H'BA80000A	H'60	LSR (LineStatusRegister)	N.A	
H'BA80000C	H'X0	MSR (ModemStatusRegister)	N.A	
H'BA80000E	H'FF	SPR (ScratchpadRegister)	SPR (ScratchpadRegister)	

5.4 LCD

5.4.1 Block Description

Figure 5.6 shows the LCD control block. As shown in Figure 5.6, the LCD control block contains an internal LCD controller and an LCD panel (TFT liquid crystal panel) mounted on the LCD board that can display 16-bit RGB data with a resolution of QVGA (240 x 320). In addition, the SRAM with an internal LCD controller is used for the LCD display VRAM (Video RAM).

Display data is stored in the internal SDRAM of the LCD controller in the order of coordinates (0,0), (1,0), … and (239, 319) from the address set in the register (LDSARU) of the LCD controller. On the LCD panel display, data at the upper left corner is handled as data on the origin (0,0) and data at the lower right corner is handled as data on the coordinates (239,319).

The front light on the LCD panel can be turned on or off by the power supply controller. For details on front light control, refer to 6. "Power Supply Controller." In addition, refer to the pertinent SH7760 Hardware Manual for details on the LCD controller.

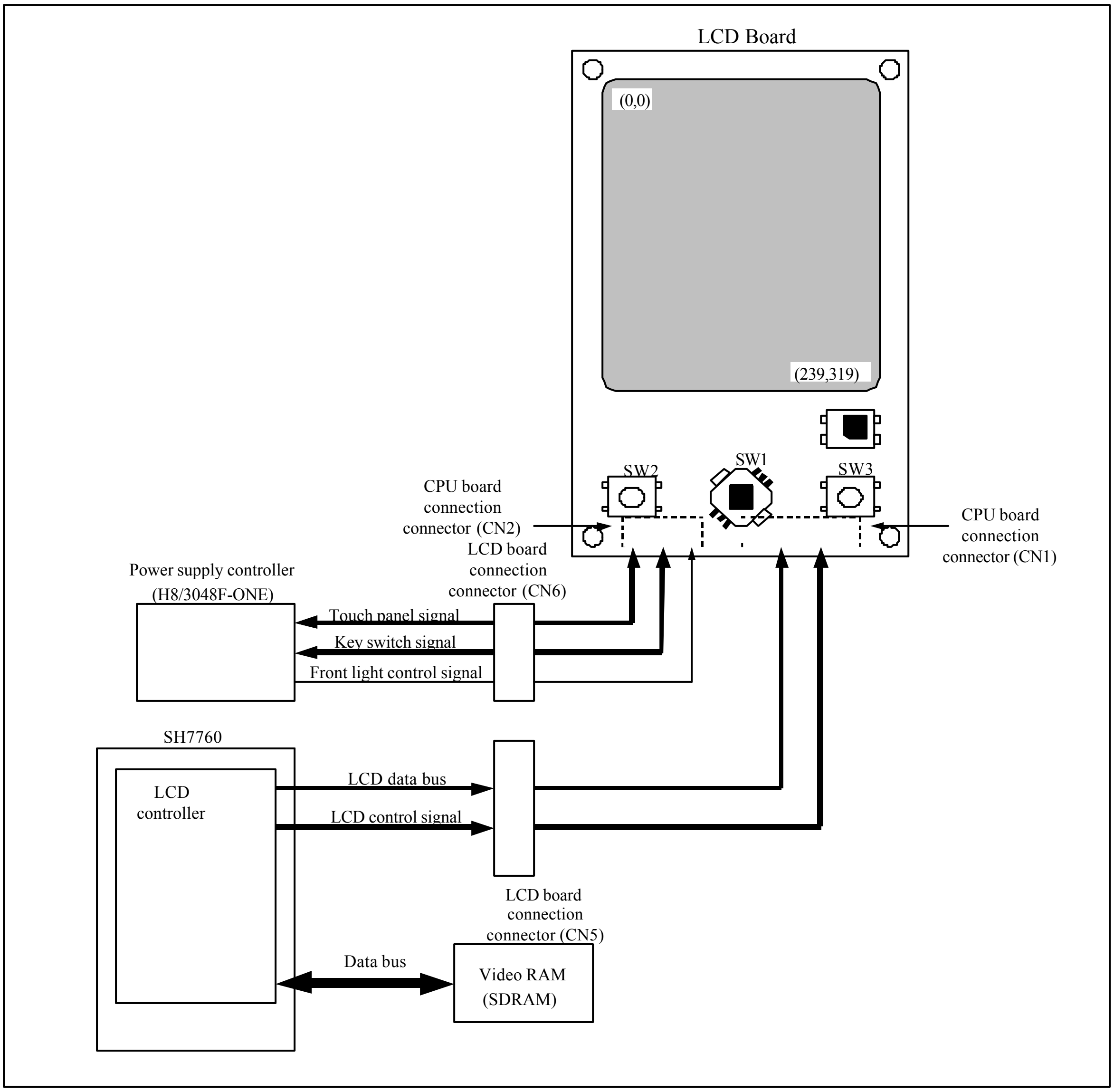


Figure 5.6 LCD Control Block

5.4.2 Connector Pins

Figure 5.7 shows the pins of the LCD interface connectors (CN5 and CN6). Tables 5.6 and 5.7 summarize the signals of these interface connectors.

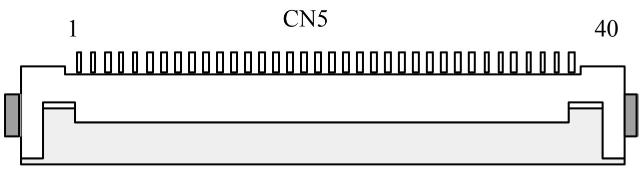


Figure 5.7 LCD Interface Connector (CN5/CN6) Pins

Table 5.6 LCD Interface Connector (CN5) Signals

Pin No.	Signal name	I/O	Remarks	Pin No.	Signal name	I/O	Remarks
1	VBAT	-	Power supply	21	LCD13	OUT	LCDC
2	VBAT	-	Power supply	22	LCD14	OUT	LCDC
3	VBAT	-	Power supply	23	LCD15	OUT	LCDC
4	VBAT	-	Power supply	24	GND	-	Power supply
5	N.C	-	Unused	25	GND	-	Power supply
6	LCD0	OUT	LCDC	26	CL1	OUT	LCDC
7	LCD1	OUT	LCDC	27	CL2	OUT	LCDC
8	LCD2	OUT	LCDC	28	DON	OUT	LCDC
9	LCD3	OUT	LCDC	29	M_DISP	OUT	LCDC
10	LCD4	OUT	LCDC	30	FLM	OUT	LCDC
11	LCD5	OUT	LCDC	31	VEPWC	OUT	LCDC
12	LCD6	OUT	LCDC	32	VCPWC	OUT	LCDC
13	LCD7	OUT	LCDC	33	NC	-	Unused
14	GND	-	Power supply	34	GND	-	Power supply
15	GND	-	Power supply	35	GND	-	Power supply
16	LCD8	OUT	LCDC	36	IR_IN	IN	Remote control
17	LCD9	OUT	LCDC	37	3.3V	-	Power supply
18	LCD10	OUT	LCDC	38	3.3V	-	Power supply
19	LCD11	OUT	LCDC	39	3.3V	-	Power supply
20	LCD12	OUT	LCDC	40	3.3V	-	Power supply

Table5.7 LCD Interface Connector (CN6) Signals

Pin No.	Signal name	I/O	Remarks	Pin No.	Signal name	I/O	Remarks
1	GND	-	Power supply	13	~PAD_CS	OUT	PAD I/F
2	GND	-	Power supply	14	~PAD_IRQ	IN	PAD_I/F
3	KEY_IN0	IN	KEY_I/F	15	PAD_DIN	OUT	PAD_I/F
4	KEY_IN1	IN	KEY_I/F	16	PAD_DOUT	IN	PAD_I/F
5	KEY_IN2	IN	KEY_I/F	17	PAD_DCLK	OUT	PAD_I/F
6	KEY_IN3	IN	KEY_I/F	18	~RESET	OUT	Reset
7	KEY_IN4	IN	KEY_I/F	19	~LCD_FLON	OUT	LCD power supply
8	KEY_OUT0	OUT	KEY_I/F	20	~LCD_PWRDY	IN	LCD power supply
9	KEY_OUT1	OUT	KEY_I/F	21	GND	-	Power supply
10	KEY_OUT2	OUT	KEY_I/F	22	GND	-	Power supply
11	GND	-	Power supply	23	3.3VSB	-	Power supply
12	GND	-	Power supply	24	3.3VSB	-	Power supply

5.4.3 Register Map

Table 5.8 shows a register map for the LCD controller.

Table 5.8 LCD Controller Registers

Address	Initial value	Register name
H'FE300C00	H'0101	Input clock register
H'FE300C02	H'0109	Module type register
H'FE300C04	H'000C	Data format register
H'FE300C06	H'0000	Scan mode register
H'FE300C08	H'0C000000	Starting address register for fetching upper data on the display panel
H'FE300C0C	H'0C000000	Starting address register for fetching lower data on the display panel
H'FE300C10	H'0280	Data line address offset register for fetching display data
H'FE300C12	H'0000	Palette control register
H'FE300800~ H'FE300BFC	-	Palette data register
H'FE300C14	H'4F52	Horizontal character number register
H'FE300C16	H'0050	Horizontal synchronization signal register
H'FE300C18	H'01DF	Vertical display line number register
H'FE300C1A	H'01DF	Vertical total line number register
H'FE300C1C	H'01DF	Vertical synchronization signal register
H'FE300C1E	H'000C	AC modulation signal toggle line number register
H'FE300C20	H'0000	Interrupt control register
H'FE300C24	H'0010	Power management mode register
H'FE300C26	H'F606	Power control sequence period register
H'FE300C28	H'0000	Control register

5.5 Sound Generator

5.5.1 Block Description

Figure 5.8 shows the sound generator control block. As shown in Figure 5.8, this control block contains the serial sound interface (SSI) of the SH7760 and the Audio CODEC (UDA1342TS from Philips), so that sound can be output to headphones connected to the output mini-jack (CN9) or can be input to earphones connected to the I/O mini-jack (CN10). In addition, headphone output takes place with the quality of stereo output while earphone I/O takes place with the quality of monaural I/O that uses only the Rch.

The IIC interface of the SH7760 is used for the initial setting and for modification of the Audio CODEC internal registers.

This control block is connected to an electronic volume so that sound output volume can be controlled. The electronic volume is controlled by the power supply controller. For details, refer to 6, "Power Supply Controller."

T-Engine has the following characteristics for microphone input and headphone output:

- Microphone input
  - Impedance: 2.2KΩ
  - Sensitivity: -51dB/Pa
- Headphone output
  - Impedance: 32Ω

For more details, refer to the SH7760 Hardware Manual or the Philips UDA1342TS Manual.

Philips Homepage: http://www.semiconductors.philips.com/

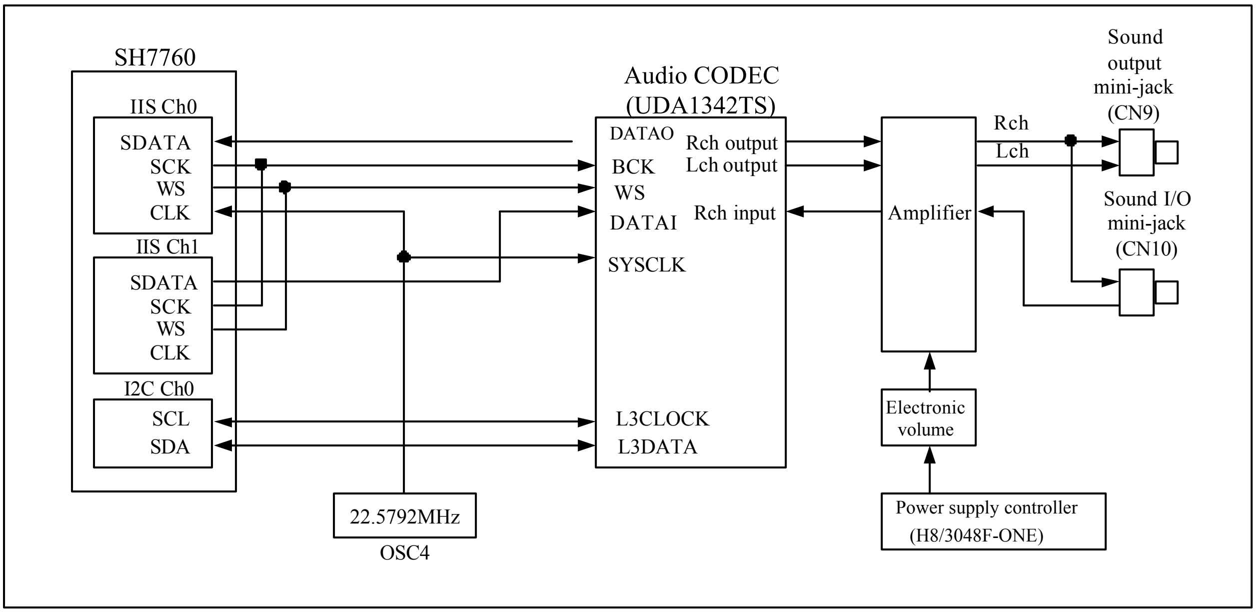
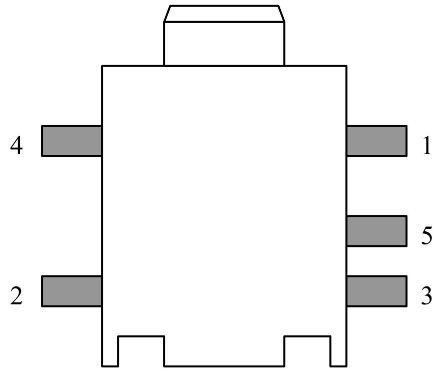


Figure 5.8 Sound Generator Control Block

5.5.2 Connector Pins

Figure 5.9 shows the pins of the sound generator I/O mini-jack (CN9, CN10). Tables 5.9 and 5.10 list the signals of the sound generator I/O mini-jack (CN9, CN10).



CN9,CN10: Sound generator I/O mini-jack (⌀2.5)
Model name: HSJ1602-010011
Maker: Hoshiden Corporation

Figure 5.9 Sound Generator I/O Mini-jack (CN9, CN10) Pins

Table 5.9 Sound Generator I/O Mini-jack (CN9) Signals

Pin No	Signal Name
1	GND
2	R-IN
3	R-OUT
4	MIC-IN
5	HP_SENSE

Table 5.10 Sound Generator I/O Mini-jack (CN10) Signals

Pin No	Signal Name
1	GND
2	L-OUT
3	R-OUT
4	HP_SENSE
5	NC

5.5.3 Register Map

Table 5.11 shows a register map for the SH7760 SSI registers.

Table 5.11 SSI Controller Register

Resister Abbreviation	Address	R/W	Initial Value	Access Size
SSICR0	H'FE680000	R/W	H'0000 0000	32
SSISR0	H'FE680004	R/W	H'0200 0003	32
SSITDR0	H'FE680008	R	H'0000 0000	32
SSIRDR0	H'FE68000C	R	H'0000 0000	32
SSICR1	H'FE690000	R/W	H'0000 0000	32
SSISR1	H'FE690004	R/W	H'0200 0003	32
SSITDR1	H'FE690008	R	H'0000 0000	32
SSIRDR1	H'FE69000C	R	H'0000 0000	32

5.6 eTRON Interface

5.6.1 Block Description

Figure 5.11 shows an eTRON interface control block. As shown in Figure 5.11, this control block contains the SIM card module of the SH7760, the power supply/level converter (LTC1555LEGN-1.8), and the 8-pin connector (CN4) to interact with the eTRON card inserted into the eTRON interface connector (CN4).

The eTRON card can be reset by controlling the SH7760 internal SIM card module register (SISCMR).
The control method is shown below.

"Low" output from PTE4: The reset pin of the eTRON card is set to "Low." (Reset state)
"High" output from PTE4: The reset pin of the eTRON card is set to "High." (Normal state)

Power supply to the eTRON card is controlled via the power supply controller (H8/3048-ONE). However, when the T-Engine board is ON, the eTRON card is being powered. When inserting or removing the eTRON card, be sure to turn off T-Engine in advance. For more information, refer to the pertinent SH7760 Hardware Manual.

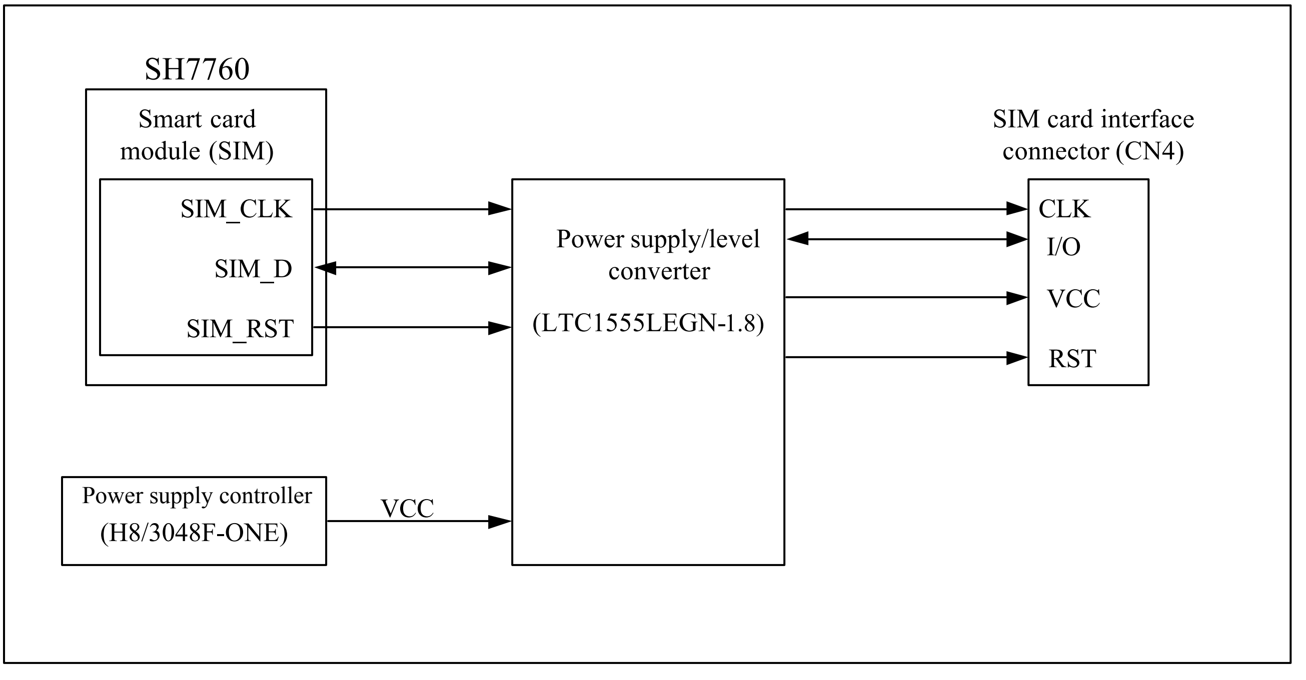


Figure 5.11 eTRON Interface Control Block

5.6.2 Connector Pins

Figure 5.12 shows the pins of the SIM card interface connector (CN4). Table 5.12 summarizes the signals of the SIM card interface connector (CN4).

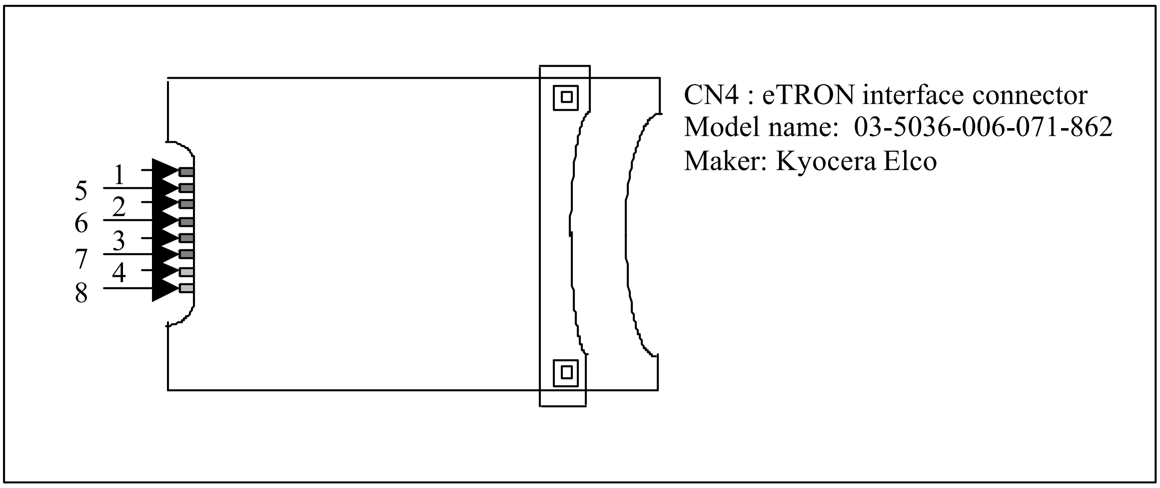


Figure 5.12 eTRON Interface Connector (CN4) Pins

Table 5.12 eTRON Interface Connector (CN4) Signals

Pin No	Signal Name
1	C1:VCC
2	C2:RST
3	C3:CLK
4	C4:*1
5	C5:GND
6	C6:VPP
7	C7:I/O
8	C8: *1

*1: Pins 4 and 8 are connected to the connector (CN13) for board test. Don't use this connector for the other purpose.

5.6.3 Register Map

Table 5.13 shows a register map for the SH7760 SIM card module (SIM).

Table 5.13 SIM Card Module Register Map

Address	Initial value	Register name
H'FE480000	H'20	Serial mode register
H'FE480002	H'07	Bit rate register
H'FE480004	H'00	Serial control register
H'FE480006	H'FF	Transmit data register
H'FE480008	H'84	Serial status register
H'FE48000A	H'00	Receive data register
H'FE48000C	H'01	Smart card mode register
H'FE48000E	H'00	Serial control 2 register
H'FE480010	H'0000	Wait time register
H'FE480012	H'00	Guard extension register
H'FE480014	H'0173	Sample register

5.7 I/O Board

5.7.1 Block Description

Figure 5.13 shows the control block of an I/O board. As shown in Figure 5.13, the SH7760 module pins output signals to the connectors (through-holes), which provide various interfaces with the external device.

As the connector is not installed, when an external pin is to be connected, it should be directly connected to the through-hole, or the connector should be installed.

The internal modules, which output the signals, are listed below.

Hitachi controller area network 2 (HCAN2): 2ch

Serial communication interface (SCIF): 2ch

IIC bus interface: 1ch

A/D converter: 4ch

Compare match timer (CMT)

For details on each module, refer to the pertinent SH7760 Hardware Manual.

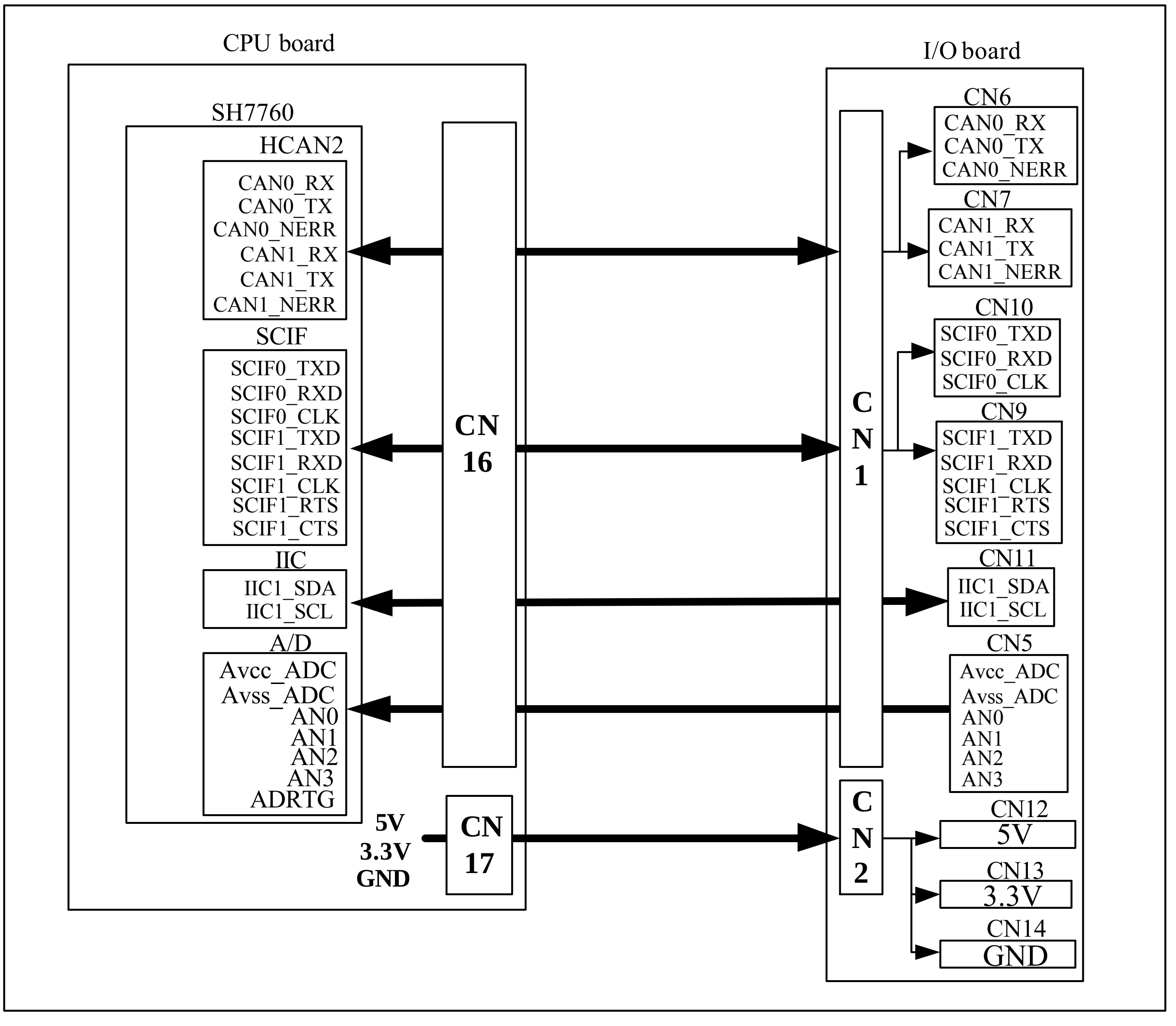


Figure 5.13 I/O Board Control Block

5.7.2 Connector (Through-Hole) Pin Assignments

Tables 5.14 to 5.22 show the connector (through-hole) pin assignments on the I/O board.

Table 5.14 A/D Converter I/F Connector (CN5) Pin Assignments

Pin No.	Signal Name
1	AVcc ADC
2	AN3
3	AN2
4	AN1
5	AN0
6	AVss_ADC

Table 5.15 HCAN2 I/F Connector (CN6) Pin Assignments

Pin NO.	Signal Name
1	CAN0_TX
2	CAN0_RX
3	CAN0_NERR

Table 5.16 HCAN2 I/F Connector (CN7) Pin Assignments

Pin No.	Signal Name
1	CAN1_TX
2	CAN1_RX
3	CAN1_NERR

Table 5.17 CMT I/F Connector (CN8) Pin Assignments

Pin No.	Signal Name
1	CMT_CTR0
2	CMT_CTR1
3	CMT_CTR2
4	CMT_CTR3

Table 5.18 SCIF Connector (CN9) Pin Assignments

Pin NO.	Signal Name
1	SCIF1_TXD
2	SCIF1_RXD
3	SCIF1_RTS
4	SCIF1_CTS
5	SCIF1_CLK

Table 5.19 SCIF Connector (CN10) Pin Assignments

Pin No.	Signal Name
1	SCIF0_TXD
2	SCIF0_RXD
3	SCIF0_CLK

Table 5.20 5V Power Supply Connector (CN6) Pin Assignments

Pin No.	Signal Name
1	5V
2	5V
3	5V
4	5V

Table 5.21 3.3V Power Supply Connector (CN6) Pin Assignments

Pin NO.	Signal Name
1	3.3V
2	3.3V
3	3.3V
4	3.3V

Table 5.22 GND Connector (CN6) Pin Assignments

Pin No.	Signal Name
1	GND
2	GND
3	GND
4	GND

6. Power Supply Controller

6.1. Power Supply Controller Functions

The H8/3048F-ONE power supply controller (simply called the power supply controller) provides the following control functions with firmware stored in the internal memory. The following functions can be controlled through the UART ChA from the SH7760. Figure 6.1 shows a power supply controller block diagram.

(1) RTC (real-time clock) function
(2) System power supply (3.3V/5/0V) ON/OFF control function
(3) Touch panel coordinate position read function
(4) Key switch input function
(5) Infrared remote control transmission/reception function
(6) Electronic volume
(7) Serial EEPROM read/write function

These functions can be controlled through the UART chA from SH7760.

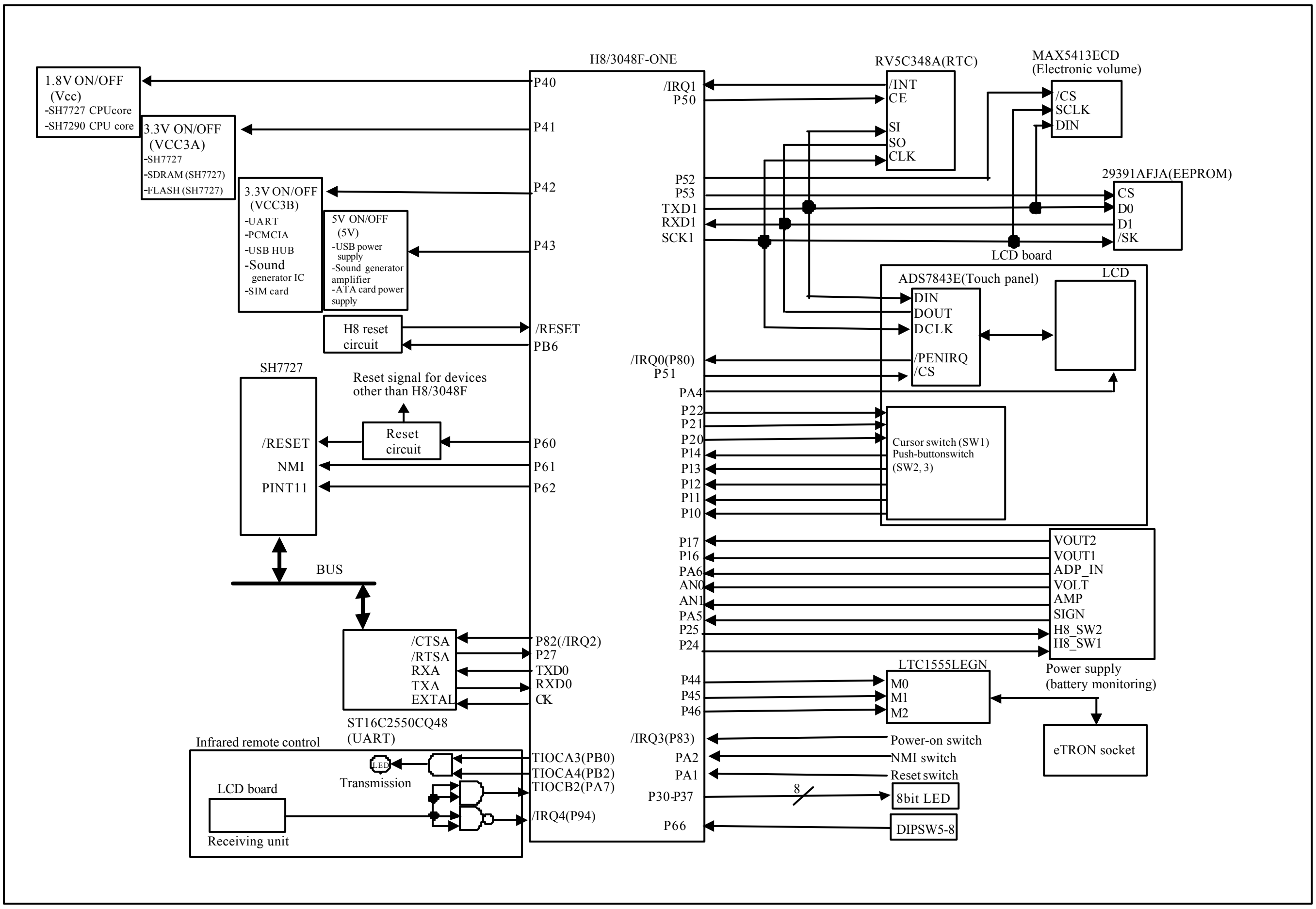


Figure 6.1 Power Supply Control Block Diagram

CAUTION

Though the power supply controller's I/O port is connected to the /RTSA and /CTSA pins of the UART controller (ST16C2550) through the circuit, the power supply controller does not execute hardware control during communications with SH7760. For details of communications between SH7760 and the power supply controller, refer to 6.2 "Serial Communications between SH7760 and the Power Supply Controller."

6.2 Serial Communications between SH7760 and the Power Supply Controller

This section describes how serial communications take place between SH7760 and the power supply controller.

6.2.1 Serial Format

This subsection describes a format for serial communications between SH7760 and the power supply controller.

(1) Mode: Start-stop

(2) Baud rate: 38400 bits/second

(3) Stop bit: 1 bit

(4) Start bit: 1 bit

(5) Parity bit: None

(6) LSB first

6.2.2 Power Supply Control Register Read Procedure

This subsection describes a procedure for reading the power supply control registers.

(1) SH7760 issues a read command to a power supply controller.

(2) The power supply controller returns a response to SH7760.

⚠ CAUTION
Don't issue multiple commands continually from SH7760. Note that the next command must be issued after a response to the preceding command has been returned from the power supply controller.

6.2.3 Read Command

Figure 6.2 shows a read command format. SH7760 sends a start code, a function code and a register address, in this order, as a read command.

(1) Start code (1 byte)	(2) Function code (1 byte or 2 bytes)	(3) Register address (2 bytes)

Figure6.2 Read Command

(1) Start code

The code is fixed at 0 x 02.

(2) Function code

- A 1-byte function code specifies the size of data to be read in the lower 4 bits when the upper 4 bits of a function code are 1000. Figure 6.3 shows a function command where the upper 4 bits are 1000.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	Size of data			

Figure6.3 Function Command (1 Byte)

- A 2-byte function code specifies the size of data to be read in the lower 12 bits when the upper 4 bits of a function code are 1001. Figure 6.4 shows a function command where the upper 4 bits are 1001.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	Size of data											

Figure6.4 Function Command (2 Bytes)

(3) Register Address

The register address specifies the address of the register to be read

6.2.4 Normal Response during a Read Operation

Figure 6.5 shows the response format for the read command. The power supply controller returns an ACK code, a function code, a register address and target data, in this order, as a response.

(1)ACK code(1 byte)	(2)Function code (1 byte or 2 bytes)	(3)Register address (2 bytes)	(4) Data (N byte)

Figure 6.5 Normal Response during a Read Operation

(1) ACK code

The code is fixed at ACK (0x06).

(2) Function code

The same function code as for the read command returns.

(3) Register address

The address of a register subject to a read operation returns.

(4) Data

Read data returns. The size of this data is equal to the value specified in the function code.

6.2.5 Error Response during a read Operation

Figure 6.6 shows the error response format for the read command. The power supply controller returns a NAK code and an error code in this order as a response at error occurrence.

(1) NAK code (1 byte)	(2) Error code (1byte)

Figure 6.6 Error Response during a Read Operation

(1) NAK code

This code is fixed at NAK (0x15).

(2) Error code

Table 6.1 summarizes the error codes.

Table 6.1 Error Codes

Error No	Error type
0x01	Communications error
0x02	Invalid function code
0x03	Invalid register number
0x04	Register size error
0x05	Data size error

6.2.6 Power Supply Control Register Write Procedure

This subsection describes the procedure for writing to a controller control of the power supply controller from SH7760.

(1) SH7760 issues a write command to the power supply controller.

(2) The power supply controller returns a response the SH7760.

⚠ CAUTION

Don't issue multiple commands continually from SH7760. Note that the next command must be issued after a response to the preceding command has been returned from the power supply controller.

6.2.7 Write Command

Figure 6.7 shows the write command format. SH7760 sends a start code, a function code, a register address and data, in this order, as a write command.

(1) Start code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2 byte)	(4) Register address (N byte)

Figure 6.7 Read Command

(1) Start code

This code is fixed at 0x02.

(2) Function code

- A 1-byte function code specifies the size of data to be written in the lower 4 bits when the upper 4 bits of a function code are 1100. Figure 6.8 shows a function command where the upper 4 bits are 1100.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	Size of data			

Figure 6.8 Function Command (1 Byte)

- A 2-byte function code specifies the size of data to be written in the lower 12 bits when the upper 4 bits of a function code are 1101. Figure 6.9 shows a function command where the upper 4 bits are 1101.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	Size of data											

Figure 6.9 Function Command (2 Bytes)

(3) Register Address

The register address specifies the address of the register to be written.

(4) Data

This field specifies the size of data to be written. This data size is equal to that specified in the function code.

6.2.8 Normal Response during a Write Operation

Figure 6.10 shows the response format for the write command. The power supply controller returns an ACK code, a function code, a register address and target data, in this order, as a response for the write command.

(1) ACK code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2 byte)	(4) Data (N byte)

Figure 6.10 Normal Response during a Write Operation

(1) ACK code

This code is fixed at ACK (0x06).

(2) Function code

The same code as for the write command returns.

(3) Register address

The address of a register subject to a write operation returns.

(4) Data

Write data returns. The size of this data is equal to the value specified in the function code. However, note that no data returns for IRRSFDR subject to infrared remote control and EEPDR subject to serial EEPROM control.

6.2.9 Error Response during a Write Operation

Figure 6.11 shows an error response format for the write command at error occurrence. The power supply controller returns a NAK code and an error code in this order as an error response.

(1) NAK code (1 byte)	(2) Error code (1 byte)

Figure 6.11 Error Response during a Write Operation

(1) NAK code

This code is fixed at NAK (0x15).

(2) Error code

Table 6.2 summarizes the error codes.

Table 6.2 Error Codes

Error Code No.	Error type
0x01	Communications error
0x02	Invalid function code
0x03	Invalid register number
0x04	Register size error
0x05	Data size error

6.3 RTC (Real-time Clock) Functions

This section describes the RTC functions. Table 6.1 summarizes the RTC registers. For a detailed description of each register, refer to 6.3.1 to 6.3.17.

(1) Function for counting the seconds, minutes, hours, day of the week, month, and year (BCD code)

(2) RTC start/stop function

(3) Alarm interrupt function

(4) 1sec/0.5sec cyclic interrupt function

(5) Automatic correction function for leap years

(6) Effective range of operation from January 1, 2000 to December 31, 2099

Table 6.3 RTC Registers

Register	Abbreviation	Address	R/W	Size	Remarks
RTC control register	RTCCR	0x0000	R/W	1 byte	
RTC status register	RTCSR	0x0001	R/W	1 byte	
Second counter	SECCNT	0x0002	R/W	1 byte	
Minute counter	MINCNT	0x0003	R/W	1 byte	
Hour counter	HRCNT	0x0004	R/W	1 byte	
Day-of-the-week counter	WKCNT	0x0005	R/W	1 byte	
Day counter	DAYCNT	0x0006	R/W	1 byte	
Month counter	MONCNT	0x0007	R/W	1 byte	
Year counter	YRCNT	0x0008	R/W	1 byte	
Second alarm counter	SECAR	0x0009	R/W	1 byte	
Minute alarm counter	MINAR	0x000A	R/W	1 byte	
Hour alarm counter	HRAR	0x000B	R/W	1 byte	
Day-of-the-week alarm counter	WKAR	0x000C	R/W	1 byte	
Day alarm counter	DAYAR	0x000D	R/W	1 byte	
Month alarm counter	MONAR	0x000E	R/W	1 byte	
RTC/Touch panel/Key input/Power supply status register	RTKISR	0x0090	R/W	1 byte	

6.3.1 RTC Control Register (RTCCR)

Address: 0x000 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CNTS	SECCAF	0.5secI	1secI	ARI	START
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) START

START bit	Setting
0	RTC start (Initial value)
1	RTC stop

CAUTION

Don't write to any counter while the START bit is set to "0." Rewrite each counter after setting the START bit to "1."

(2) ARI

ARI bit	Setting
0	No alarm interrupt is generated (Initial value)
1	An alarm interrupt is generated

(3) 1secI

1secI bit	Setting
0	No interrupt is generated at intervals of 1 second. (Initial value)
1	An interrupt is generated at intervals of 1 second.

(4) 0.5secI

0.5secI bit	Setting
0	No interrupt is generated at intervals of 0.5 second. (Initial value)
1	An interrupt is generated at intervals of 0.5 second.

(5) SECCAF

SECCAF bit	Setting
0	No carry has been generated in the second counter (SECCNT). (Initial value)
1	A carry has been generated in the second counter (SECCNT). [Zero-clear condition] The SECCAF bit is set to "1.''

(6) CNTS

CNTS bit	Setting
0	The setting (value) of each counter is not updated. (Initial value)
1	The setting (value) of each counter is updated. [Zero-clear condition] Counter update is completed. This clear operation is automatically performed.

⚠ CAUTION

Don't write to any counter while the START bit is set to "0." Set the CNTS bit to "1" after updating the value of each counter with the START bit set to "1."

6.3.2 RTC Status Register (RTCSR)

Address: 0x001 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0.5 secF	1 secF	ARF	0
R	R	R	R	R/W	R/W	R/W	R

(1) ARF

ARF bit	Setting
0	The setting of each alarm register with the AR bit set is not the same as that of each counter register (Initial value)
1	The setting of each alarm register with the AR bit set is identical to that of each counter register. At this time, an interrupt occurs if the ARI bit is set to "1.'' [Clear condition] "0'' is written with the ARF bit set to "1.''

(2) 1secF

1secF bit	Setting
0	A second has not elapsed yet (Initial value)
1	A second has elapsed. [Clear condition] "0'' is written with the 1secF bit set to "1.''

(3) 0.5secF

0.5secF bit	Setting
0	A half second has not elapsed yet. (Initial value)
1	A half second has elapsed yet. [Clear condition] "0'' is written with the 0.5secF bit set to "1.''

6.3.3 Second Counter (SECCNT)

Address: 0x002 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 second			1 second			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the minute counter.

6.3.4 Minute Counter (MINCNT)

Address: 0x0003 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			1 minutes			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the hour counter.

6.3.5 Hour Counter (HRCNT)

Address: 0x0004 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 hours		1 hours			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 23. When the value changes from 23 to 00, a carry is generated in the day counter and the day-of-the-week counter.

6.3.6 Day-of-the-Week Counter (WKCNT)

Address: 0x0005 Initial Value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Septinary incremental counter		
R	R	R	R	R	R/W	R/W	R/W

Counting takes place within a range from 0x00 to 0x06.

The following shows the correspondence between the day of the week and the value of the septinary incremental counter.

(D2.D1.D0) = (0.0.0) →Sunday

(D2.D1.D0) = (0.0.1) →Monday

(D2.D1.D0) = (0.1.0) →Tuesday

(D2.D1.D0) = (0.1.1) →Wednesday

(D2.D1.D0) = (1.0.0) →Thursday

(D2.D1.D0) = (1.0.1) →Friday

(D2.D1.D0) = (1.1.0) →Saturday

6.3.7 Day Counter (DAYCNT)

Address: 0x0006 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		1 day			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 1 to 31 (January, March, July, August, October and December), 1 to 30 (April, June, September and November), 1 to 28 (February in normal year) or 1 to 29 (February in leap year).

6.3.8 Month Counter (MONCNT)

Address: 0x0007 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	October	January			
R	R	R	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 1 to 12. When the counter value changes from 12 to 1, a carry is generated in the year counter.

6.3.9 Year Counter (YRCNT)

Address: 0x0008 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				1 year			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 0 to 99. In this range, 00, 04, ..., 92 and 96 are leap years.

6.3.10 Alarm Register

Each alarm register corresponds to the relevant counter as shown below.

If the AR bit (D7) of each alarm is set to "1," counters will be compared with alarm registers. This comparison is performed only for alarm registers with the AR bit (D7) set to "1" and an alarm interrupt is generated only at correct correspondence.

• Correspondence between the alarm registers and counters

Second alarm register (BCD code): second counter

Minute alarm register (BCD code): minute counter

Hour alarm register (BCD code): Hour counter

Day-of-the-week alarm register (0x00 to 0x07): Day-of-the-week counter

Day alarm register (BCD code): Day counter

Month alarm register (BCD code): Month counter

6.3.11 Second Alarm Register (SECAR)

Address: 0x0009 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	10 seconds			1 second			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 59.

6.3.12 Minute Alarm Register (MINAR)

Address: 0x000A Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	10 minutes			1 minute			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 59.

6.3.13 Hour Alarm Register (HRAR)

Address: 0x000B Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	10 hours		1 hour			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 23.

6.3.14 Day-of-the-Week Alarm Register (WKAR)

Address: 0x000C Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	0	0	0	Septinary counter value		
R/W	R	R	R	R	R/W	R/W	R/W

The alarm value must be set within a range from 0x00 to 0x06.

- Day of the week and septinary counter value

(D2.D1.D0) = (0.0.0) → Sunday

(D2.D1.D0) = (0.0.1) → Monday

(D2.D1.D0) = (0.1.0) → Tuesday

(D2.D1.D0) = (0.1.1) → Wednesdady

(D2.D1.D0) = (1.0.0) → Thursday

(D2.D1.D0) = (1.0.1) → Friday

(D2.D1.D0) = (1.1.0) → Saturday

6.3.15 Day Alarm Register (DAYAR)

Address: 0x000D Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	10 days		1 day			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 1 and 31 (January, March, May, July, August, October and December), between 1 and 30 (April, June, September and November), between 1 and 28 (February in normal year) or between 1 and 29 (February in leap year).

6.3.16 Month Alarm Register (MONAR)

Address: 0x000E Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	0	October	January			
R/W	R	R	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 01 and 12.

6.3.17 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel or key input status. The following is a brief description of RTC-related status bits.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) RTCIF

RTCIF bit	Setting
0	The ARF, 1secF ad 0.5secF bits of the RTC register are all set to "0.'' (Initial value)
1	One of the ARF, 1secF ad 0.5 secF bits of the RTC register is set to "1.'' [Clear condition] "0'' is written with the RTCIF bit set to ''1.''

6.4 Touch Panel Functions

This section describes the touch panel functions. In addition, Table 6.4 summarizes the touch panel registers. For details of each register, refer to 6.4.1 to 6.4.32.

(1) The A/D conversion value of the X or Y position sensed by pen touch is output.

(2) Pen touch ON/OFF interrupt function

Sampling takes place at intervals of 20msec to 100msec. When the results (A/D conversion value of the X or Y position) obtained three times from sampling are approximate to each other, a pen touch ON interrupt is generated for SH7760. In addition, when the touch panel is turned off, a pen touch OFF interrupt is generated.

(3) To keep the pen touch "ON," sampling is performed at intervals of 20msec to 100msec and a pen touch ON interrupt is generated if the results obtained from sampling are approximate to each other.

(4) Calibration function

Calibration is performed when two points on the touch panel are touched with the pen.

After completion of calibration, the X and Y positions are converted into the LCD drawing dot positions for output.

Table 6.4 Touch Panel Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Touch panel control register	TPLCR	0x0020	R/W	1 byte	
Touch panel status register	TPLSR	0x0021	R/W	1 byte	
Touch panel sampling control register	TPLSCR	0x0022	R/W	1 byte	
X position A/D register	XPAR	0x0024	R	2 bytes	
Y position A/D register	YPAR	0x0026	R	2 bytes	
X position dot register	XPDR	0x0028	R	2 bytes	
Y position dot register	YPDR	0x002A	R	2 bytes	
XA position dot register	XAPDR	0x002C	R/W	2 bytes	
YA position dot register	YAPDR	0x002E	R/W	2 bytes	
XB position dot register	XBPDR	0x0030	R/W	2 bytes	
YB position dot register	YBPDR	0x0032	R/W	2 bytes	
XC position dot register	XCPDR	0x0034	R/W	2 bytes	
YC position dot register	YCPDR	0x0036	R/W	2 bytes	
XA position A/D register	XAPAR	0x0038	R/W	2 bytes	
YA position A/D register	YAPAR	0x003A	R/W	2 bytes	
XB position A/D register	XBPAR	0x003C	R/W	2 bytes	
YB position A/D register	YBPAR	0x003E	R/W	2 bytes	
XC position A/D register	XCPAR	0x0040	R/W	2 bytes	
YC position A/D register	YCPAR	0x0042	R/W	2 bytes	
DX dot register	DXDR	0x0044	R/W	2 bytes	
DY dot register	DYDR	0x0046	R/W	2 bytes	
X position dot calculation A/D value	XPARDOT	0x0048	R/W	2 bytes	
X position A/D value 1	XPARDOT1	0x004A	R/W	2 bytes	
X position A/D value 2	XPARDOT2	0x004C	R/W	2 bytes	
X position A/D value 3	XPARDOT3	0x004E	R/W	2 bytes	
X position A/D value 4	XPARDOT4	0x0050	R/W	2 bytes	
Y position dot calculation A/D value	YPARDOT	0x0052	R/W	2 bytes	
Y position A/D value 1	YPARDOT1	0x0054	R/W	2 bytes	
Y position A/D value 2	YPARDOT2	0x0056	R/W	2 bytes	
Y position A/D value 3	YPARDOT3	0x0058	R/W	2 bytes	
Y position A/D value 4	YPARDOT4	0x005A	R/W	2 bytes	
RTC/Touch Panel/Key Input/Power Supply Status Register	RTKISR	0x0090	R/W	1 byte	

6.4.1 Touch Panel Control Register (TPLCR)

Address: 0x0020 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PEN_ONRE	PEN_OFFI	PEN_ONI	TP_STR
R	R	R	R	R/W	R/W	R/W	R/W

(1) TP_STR

TP_STR bit	Setting
0	The touch panel is disabled. (Initial value)
1	The touch panel is enabled.

(2) PEN_ONI

PEN_ONI bit	Setting
0	A pen touch ON interrupt is not generated. (Initial value)
1	A pen touch ON interrupt is generated.

(3) PEN_OFFI

PEN_OFFI bit	Setting
0	A pen touch OFF interrupt is not generated. (Initial value)
1	A pen touch OFF interrupt is generated.

(4) PEN_ONRE

PEN_ ONRE bit	Setting
0	A pen touch ON interrupt is not generated when pen touch continues. (Initial value)
1	A pen touch ON interrupt is generated when pen touch continues.

6.4.2 Touch Panel Status Register (TPLSR)

Address: 0x0021 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	PEN_OFFIF	PEN_ONIF	0
R	R	R	R	R	R/W	R/W	R

(1) PEN_ONIF

PEN_ONIF bit	Setting
0	The touch panel has not been pen-touched. (pen touch OFF.) (Initial value)
1	The pen-touch state on the touch panel has been changed from OFF to ON. The touched positions on the touch panel are output to the X position A/D register, Y position A/D register, X position dot register and Y position dot register. At this time, a pen touch ON interrupt is generated if the PEN_ONI bit is set to "1." [Clear condition] "0" is written with the PEN_ONIF bit set to "1."

(2) PEN_OFFIF

PEN_OFFIF bit	Setting
0	The touch panel has not been pen-touched. (pen touch OFF.) (Initial value)
1	The pen-touch state on the touch panel has been changed from ON to OFF. At this time, a pen touch OFF interrupt is generated if the PEN_OFFI bit is set to "1." [Clear condition] "0" is written with the PEN_OFFIF bit set to "1."

6.4.3 Touch panel Sampling Control Register (TPLSCR)

The touch panel sampling control register sets a sampling interval for the touch panel.

Address: 0x0022 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
160msec	140msec	120msec	100msec	80msec	60msec	40msec	20msec
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

A sampling interval for the touch panel can be set within a range from 20msec to 160msec (unit: 20msec). When a bit is set to "1," the corresponding sampling interval from 20msec to 160msec is set. Note that only the following values can be specified.

- Correspondence between the setting values and sampling intervals

  0x01: 20msec

  0x02: 40msec

  0x04: 60msec

  0x08: 80msec

  0x10: 100msec

  0x20: 120msec

  0x40: 140msec

  0x80: 160msec

6.4.4 X Position A/D Register (XPAR)

Address: 0x0024 Initial value: 0x000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XA_D11	XA_D10	XA_D9	XA_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
XA_D7	XA_D6	XA_D5	XA_D4	XA_D3	XA_D2	XA_D1	XA_D0
R	R	R	R	R	R	R	R

The X position A/D register indicates the A/D conversion result of a pen-touched X position on the touch panel.

6.4.5 Y Position A/D Register (YPAR)

Address: 0x0026 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YA_D11	YA_D10	YA_D9	YA_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
YA_D7	YA_D6	YA_D5	YA_D4	YA_D3	YA_D2	YA_D1	YA_D0
R	R	R	R	R	R	R	R

The Y position A/D register indicates the A/D conversion result of a pen-touched Y position on the touch panel.

6.4.6 X Position Dot Register (XPDR)

Address: 0x0028 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XD_D15	XD_D14	XD_D13	XD_D12	XD_D11	XD_D10	XD_D9	XD_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
XD_D7	XD_D6	XD_D5	XD_D4	XD_D3	XD_D2	XD_D1	XD_D0
R	R	R	R	R	R	R	R

The X position dot register indicates the dot position of a pen-touched X position on the touch panel. Use the output value of this register after calibration. The output value is not settled without calibration.

6.4.7 Y Position Dot Register (YPDR)

Address: 0x002A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YD_D15	YD_D14	YD_D13	YD_D12	YD_D11	YD_D10	YD_D9	YD_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
YD_D7	YD_D6	YD_D5	YD_D4	YD_D3	YD_D2	YD_D1	YD_D0
R	R	R	R	R	R	R	R

The Y position dot register indicates the dot position of a pen-touched Y position on the touch panel. Use the output value of this register after calibration. The output value is not settled without calibration.

6.4.8 XA Position Dot Register (XAPDR)

Address: 0x002C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XAD_D15	XAD_D14	XAD_D13	XAD_D12	XAD_D11	XAD_D10	XAD_D9	XAD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XAD_D7	XAD_D6	XAD_D5	XAD_D4	XAD_D3	XAD_D2	XAD_D1	XAD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XA position dot register indicates the X dot position of point A when calibration takes place.

6.4.9 YA Position Dot Register (YAPDR)

Address: 0x002E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YAD_D15	YAD_D14	YAD_D13	YAD_D12	YAD_D11	YAD_D10	YAD_D9	YAD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YAD_D7	YAD_D6	YAD_D5	YAD_D4	YAD_D3	YAD_D2	YAD_D1	YAD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YA position dot register indicates the Y dot position of point A when calibration takes place.

6.4.10 XB Position Dot Register (XBPDR)

Address: 0x0030 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XBD_D15	XBD_D14	XBD_D13	XBD_D12	XBD_D11	XBD_D10	XBD_D9	XBD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XBD_D7	XBD_D6	XBD_D5	XBD_D4	XBD_D3	XBD_D2	XBD_D1	XBD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XB position dot register indicates the X dot position of point B when calibration takes place.

6.4.11 YB Position Dot Register (YBPDR)

Address: 0x0032 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YBD_D15	YBD_D14	YBD_D13	YBD_D12	YBD_D11	YBD_D10	YBD_D9	YBD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YBD_D7	YBD_D6	YBD_D5	YBD_D4	YBD_D3	YBD_D2	YBD_D1	YBD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YB position dot register indicates the Y dot position of point B when calibration takes place.

6.4.12 XC Position Dot Register (XCPDR)

Address: 0x0034 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XCD_D15	XCD_D14	XCD_D13	XCD_D12	XCD_D11	XCD_D10	XCD_D9	XCD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XCD_D7	XCD_D6	XCD_D5	XCD_D4	XCD_D3	XCD_D2	XCD_D1	XCD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XC position dot register indicates the X dot position of point C when calibration takes place. This register will be functionally enhanced in future. Don’t access this register.

6.4.13 YC Position Dot Register (YCPDR)

Address: 0x0036 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YCD_D15	YCD_D14	YCD_D13	YCD_D12	YCD_D11	YCD_D10	YCD_D9	YCD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YCD_D7	YCD_D6	YCD_D5	YCD_D4	YCD_D3	YCD_D2	YCD_D1	YCD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YC position dot register indicates the Y dot position of point C where calibration takes place. This register will be functionally enhanced in future. Don’t access this register.

6.4.14 XA Position A/D Register (XAPAR)

Address: 0x0038 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XAA_D11	XAA_D10	XAA_D9	XAA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XAA_D7	XAA_D6	XAA_D5	XAA_D4	XAA_D3	XAA_D2	XAA_D1	XAA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XA position A/D register indicates the X position A/D conversion result of point A subject to calibration/

6.4.15 YA Position A/D Register (YAPAR)

Address: 0x003A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YAA_D11	YAA_D10	YAA_D9	YAA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YAA_D7	YAA_D6	YAA_D5	YAA_D4	YAA_D3	YAA_D2	YAA_D1	YAA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YA position A/D register indicates the Y position A/D conversion result of point A subject to calibration.

6.4.16 XB Position A/D Register (XBPAR)

Address: 0x003C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XBA_D11	XBA_D10	XBA_D9	XBA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XBA_D7	XBA_D6	XBA_D5	XBA_D4	XBA_D3	XBA_D2	XBA_D1	XBA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XB position A/D register indicates the X position A/D conversion result of point B subject to calibration.

6.4.17 YB Position A/D Register (YBPAR)

Address: 0x003E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YBA_D11	YBA_D10	YBA_D9	YBA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YBA_D7	YBA_D6	YBA_D5	YBA_D4	YBA_D3	YBA_D2	YBA_D1	YBA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YB position A/D register indicates the Y position A/D conversion result of point B subject to calibration.

6.4.18 XC Position A/D Register (XCPAR)

Address: 0x0040 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XCA_D11	XCA_D10	XCA_D9	XCA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XCA_D7	XCA_D6	XCA_D5	XCA_D4	XCA_D3	XCA_D2	XCA_D1	XCA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XC position A/D register indicates the X position A/D conversion result of point C subject to calibration. This register will be functionally enhanced in future. Don't access this register.

6.4.19 YC Position A/D Register (YCPAR)

Address: 0x0042 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YCA_D11	YCA_D10	YCA_D9	YCA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YCA_D7	YCA_D6	YCA_D5	YCA_D4	YCA_D3	YCA_D2	YCA_D1	YCA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YC position A/D register indicates the Y position A/D conversion result of point C subject to calibration.
This register will be functionally enhanced in future. Don't access this register.

6.4.20 DX Dot Register (DXDR)

Address: 0x0044 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
DX1_D15	DX1_D14	DX1_D13	DX1_D12	DX1_D11	DX1_D10	DX1_D9	DX1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
DX1_D7	DX1_D6	DX1_D5	DX1_D4	DX1_D3	DX1_D2	DX1_D1	DX1_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DX dot register holds a value obtained by multiplying the number of dots per data (X position A/D conversion result at calibration) by 1,000. The power supply controller outputs a dot position of the X position to be stored in the X position dot register (XPDR) from the values set in the DX dot register (DXDR), XA position dot register (XAPDR) and XA position A/D register (XAPAR). When the DX dot register (DXDR) has been set to "0," the dot position is not calculated.

6.4.21 DY Dot Register (DYDR)

Address: 0x0046 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
DY1_D15	DY1_D14	DY1_D13	DY1_D12	DY1_D11	DY1_D10	DY1_D9	DY1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
DY1_D7	DY1_D6	DY1_D5	DY1_D4	DY1_D3	DY1_D2	DY1_D1	DY1_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DY dot register (DY1DR) holds a value obtained by multiplying the number of dots per data (Y position A/D conversion result at calibration) by 1,000. The power supply controller outputs a dot position of the Y position to be stored in the Y position dot register (YPDR) from the values set in the DY dot register (DYDR), YA position dot register (YAPDR) and YA position A/D register (YAPAR). When the DY dot register (DY1DR) has been set to "0," the dot position is not calculated.

6.4.22 X Position Dot Calculation A/D Value (XPARDOT)

Address: 0X0048 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD_D9	XD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD_D7	XD_D6	XD_D5	XD_D4	XD_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value register (XPARDOT) holds an AD value of X position dot calculation. This A/D value is obtained by calculating the mean of the previous four XPARDOT values and clearing the low order 3 bits with zeros.

6.4.23 X Position Dot Calculation A/D Value 1 (XPARDOT1)

Address: 0x004A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD1_D9	XD1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD1_D7	XD1_D6	XD1_D5	XD1_D4	XD1_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 1 register (XPARDOT1) holds an XPARDOT value before sampling.

6.4.24 X Position Dot Calculation A/D Value 2 (XPARDOT2)

Address: 0x004C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD2_D9	XD2_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD2_D7	XD2_D6	XD2_D5	XD2_D4	XD2_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 2 register (XPARDOT2) holds an XPARDOT value before sampling.

6.4.25 X Position Dot Calculation A/D Value 3 (XPARDOT3)

Address: 0x004E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD3_D9	XD3_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD3_D7	XD3_D6	XD3_D5	XD3_D4	XD3_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 3 register (XPARDOT3) holds an XPARDOT value before sampling.

6.4.26 X Position Dot Calculation A/D value 4 (XPARDOT4)

Address: 0x0050 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD4_D9	XD4_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD4_D7	XD4_D6	XD4_D5	XD4_D4	XD4_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 4 register (XPARDOT4) holds an XPARDOT value before sampling.

6.4.27 Y Position Dot Calculation A/D Value (YPARDOT)

Address: 0x0052 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD_D9	YD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD_D7	YD_D6	YD_D5	YD_D4	YD_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value register (YPARDOT) holds an A/D value of Y position dot calculation. This A/D value is obtained by calculating the mean of the previous four YPARDOT values and clearing the following 3 bits with zeros.

6.4.28 Y Position Dot Calculation A/D Value 1 (YPARDOT1)

Address: 0 x0054 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD1_D9	YD1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD1_D7	YD1_D6	YD1_D5	YD1_D4	YD1_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 1 register (YPARDOT1) holds a YPARDOT value before sampling.

6.4.29 Y Position Dot Calculation A/D Value 2 (YPARDOT2)

Address: 0x0056 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD2_D9	YD2_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD2_D7	YD2_D6	YD2_D5	YD2_D4	YD2_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 2 register (YPARDOT2) holds a YPARDOT value before sampling.

6.4.30 Y Position Dot Calculation A/D Value 3 (YPARDOT3)

Address: 0x0058 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD3_D9	YD3_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD3_D7	YD3_D6	YD3_D5	YD3_D4	YD3_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 3 register (YPARDOT3) holds a YPARDOT value before sampling.

6.4.31 Y Position Dot Calculation A/D Value 4 (YPARDOT4)

Address: 0x005A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD4_D9	YD4_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD4_D7	YD4_D6	YD4_D5	YD4_D4	YD4_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 4 register (YPARDOT4) holds a YPARDOT value before sampling.

6.4.32 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits related to the touch panel.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) TPIF

TPIF bit	Setting
0	The PEN_ONIF, PEN_OFFIF, CAIF and CAEF bits of the touch panel status registered are all set to "0.'' (Initial value)
1	One of the PEN_ONIF, PEN_OFFIF, CAIF and CAEF bits of the touch panel status register is set to "1.'' [Clear condition] "0'' is written with the TPIF bit set to "1.''

6.4.33 Touch Panel Calibration Method (2-point System)

The power supply controller supports 2-point touch panel calibration. Figure 6.11shows the points of the drawing coordinates and A/D conversion coordinates that are necessary for calibration.

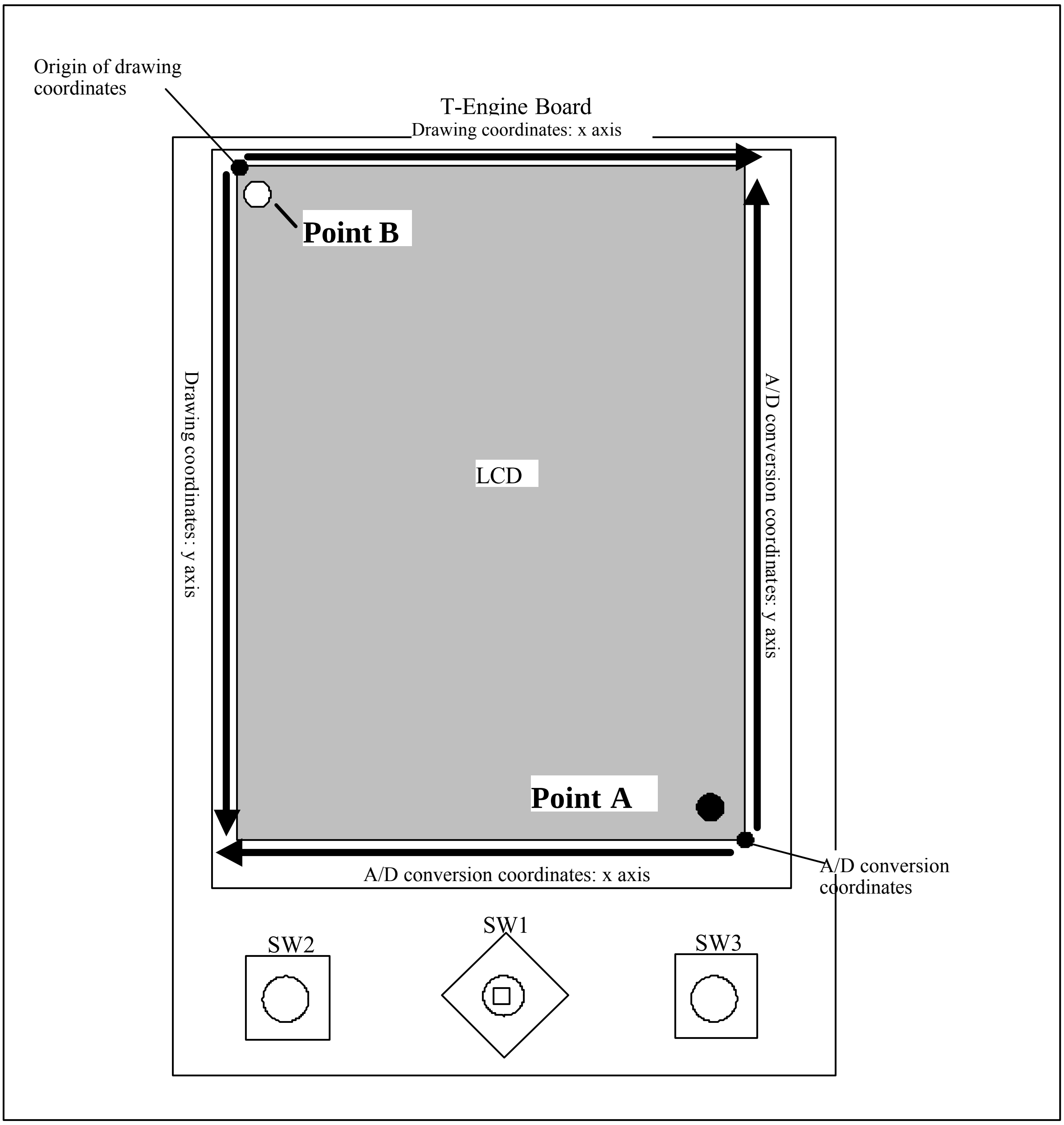


Figure 6.11 Points of the Drawing Coordinates and A/D Conversion Coordinates

[Calibration Method]

(1) The SH7760 writes the dot points of points A and B to the registers XAPDR, YAPDR, XBPDR, and YBPDR.

(2) When point A is pen-touched, it is signaled by a pen touch interrupt. The A/D conversion result of the pen-touched point A is written to the registers XAPAR and YAPAR.

(3) Next, when point B is pen-touched, it is signaled by a pen touch interrupt. The A/D conversion result of the pen-touched point B is written to the registers XBPAR and YBPAR.

(4) Calibration takes place according to data in the above steps (1) to (3). Using the following expression, the SH7760 calculates the number of dots per data of the X position A/D conversion result and that of the Y position A/D conversion result.

Number of dots per data of the X position A/D conversion result (DX)

DX = (DXA – DXB) / (TXB – TXA) Where TXA < TXB, DXA > DXB

Number of dots per data of the Y position A/D conversion result (DY)

DY = (DYA – DYB) / (TYB- TYA) Where TYA < TYB, DYA > DYB

DXA: X position drawing dot point of point A (XAPDR)
DXB: X position drawing dot point of point B (XBPDR)
TXA: X position A/D conversion result of point A (XAPAR)
TXB: X position A/D conversion result of point B (XBPAR)
DYA: Y position drawing dot point of point A (YAPDR)
DYB: Y position drawing dot point of point B (YBPDR)
TXA: Y position A/D conversion result of point A (YAPAR)
TXB: Y position A/D conversion result of point B (YBPAR)

(5) The above calculation results are multiplied by 1,000, their decimal places are rounded, and the resulting integers are written to the registers DXDR and DYDR.

DX dot register (DXDR) = DX x 1,000 (rounding the decimal places)

DY dot register (DYDR) = DY x 1,000 (rounding the decimal places)

(6) The power supply controller uses data stored in the registers DXDR, DYDR, XAPDR, YAPDR, XAPAR, and YAPAR to calculate dot position data (XPDR, YPDR) of the pen-touched point on the LCD. The power supply controller uses the following expression to calculate dot position data.

X position dot register (XPDR)
XPDR = (DXA – (DX x (TXD – TXA)) / 1,000
Y position dot register (YPDR)
YPDR = (DYA – (DY x (TYD – TYA)) / 1,000

DXA: XA position dot register (XAPDR) data
DX: DX1 dot register (DXDR) data
TXA: XA position A/D register (XAPAR) data
TXD: X position A/D register (XPAR) data
DYA: YA position dot register (YAPDR) data
DY: DY dot register (DYDR) data
TYA: YA position A/D register (YAPAR) data
TYD: X position A/D register (YPAR) data

The power supply controller outputs data stored in the X position A/D register (XPAR) and Y position A/D register (YPAR). When the values stored in the DX dot register (DXDR) and DY dot register (DYDR) are not 0, the power supply controller outputs the data derived from the above expressions to the X position dot register (XPDR) and Y position dot register (YPDR). When either value is 0, it does not use the above expression for calculation and outputs only XPAR and YPAR data.

6.5 Key Switch Control

Figure 6.12 shows the T-Engine switches under control by the power supply controller. The power supply controller controls the switches SW1 to SW3 on the CPU board and the switches SW1to SW3 on the LCD board.

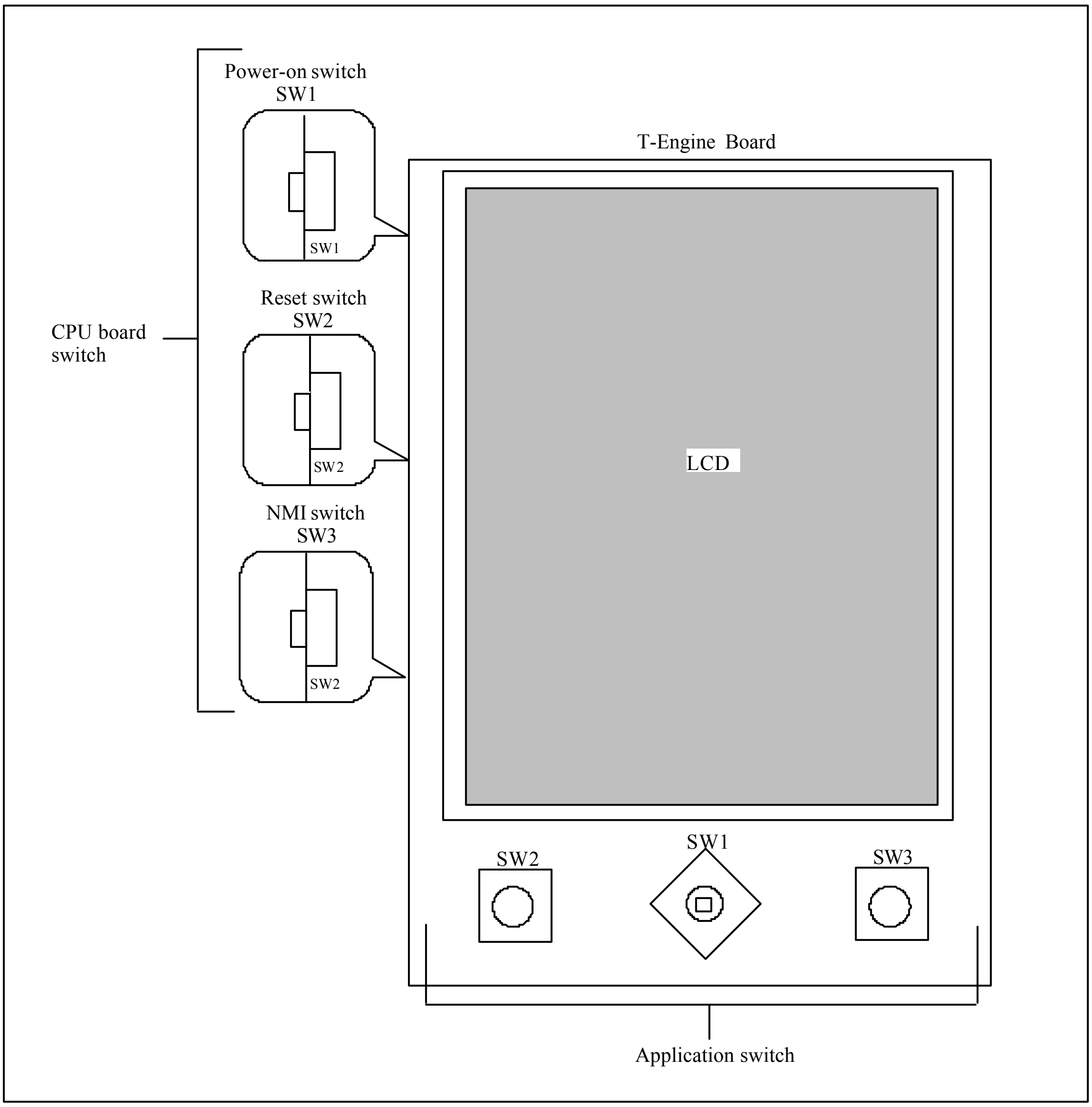


Figure 6.12 T-Engine Switch

6.5.1 CPU Board Switch Control

(1) Power-on switch (SW1)

- When the SH7760 is being powered, a power-on switch interrupt occurs for the SH7760 if the power-on switch is pressed and held for 2 seconds or more.
- When T-Engine is OFF, it is turned ON if the power-on switch is pressed and held for 0.5 seconds or more.
- When T-Engine is ON, it is turned OFF if the power-on switch is pressed and held for 2 seconds or more.

(2) Reset switch (SW2)

T-Engine is turned OFF when the reset switch is pressed.

(3) NMI switch (SW3)

An NMI interrupt occurs for the SH7760 when the NMI switch is pressed.

6.5.2 LCD Board Switch Control (Application Switch)

(1) Cursor switch (SW1) and push-button switches (SW2 and SW3) on the LCD board

- The cursor switch and push-button switches are subject to sampling at intervals of 10msec. When consecutive three samplings indicate that the same key is being pressed, key bit pattern data of the cursor switch and push-button switches are output.
- If the switch is turned ON, a key ON interrupt occurs. If the switch is turned OFF, a key OFF interrupt occurs.
- When the same switch is pressed and held, an auto repeat interrupt occurs at intervals of 100 to 450msec (unit: 50msec).

6.5.3 Key Switch Registers

Table 6.5 summarizes the key switch registers. For details of each register, refer to 6.5.4 to 6.5.8.

Table 6.5 Key Switch Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Key control register	KEYCR	0x0060	R/W	1 byte	
Key auto repeat time register	KATIMER	0x0061	R/W	1 byte	
Key bit pattern register	KBITPR	0x0064	R/W	2 bytes	
Key input status register	KEYSR	0x0062	R/W	1 byte	
RTC/Touch panel/key input/Power supply status register	RTKISR	0x0090	R/W	1 byte	

6.5.4 Key Control Register (KEYCR)

Address: 0x0060 Initial value: 0x20

D7	D6	D5	D4	D3	D2	D1	D0
0	0	NMIE	PONSWI	ARKEYI	KEY_OFFI	KEY_ONI	KEY_STR
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) KEY_STR

KEY_STR bit	Setting
0	An application switch key input is disabled. (Initial value)
1	An application switch key input is enabled.

(2) KEY_ONI

KEY_ONI bit	Setting
0	An application switch ON interrupt is disabled. (Initial value)
1	An application switch key ON interrupt is enabled.

(3) KEY_OFFI

KEY_OFFI bit	Setting
0	An application switch OFF interrupt is disabled. (Initial value)
1	An application switch key OFF interrupt is enabled.

(4) ARKEYI

ARKEYI bit	Setting
0	An application switch auto repeat interrupt is disabled. (Initial value)
1	An application switch auto repeat interrupt is enabled.

(5) PONSWI

PONSWI bit	Setting
0	A power-on switch interrupt is disabled. (Initial value)
1	A power-on switch interrupt is enabled.

(6) NMIE

NMIE bit	Setting
0	An NMI interrupt is disabled for the SH7760 even when the NMI switch is pressed.
1	An NMI interrupt is disabled for the SH7760 when the NMI switch is pressed. (Initial value)

6.5.5 Key Auto Repeat Time Register (KATIMER)

Address: 0x0061 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
450msec	400msec	350msec	300msec	250msec	200msec	150msec	100msec
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register sets the auto repeat interrupt generation time. The auto repeat interrupt generation time is set at intervals of 100msec to 450msec (unit: 50msec). When one of the bits (100msec to 450msec) is set, the corresponding auto repeat interrupt generation time is set.

6.5.6 Key Bit Pattern Register (KBIPR)

Address: 0x0064 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	SW2	0	SW3
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	SW1-5 (Decided)	SW1-4 (↓)	SW1-3 (↑)	SW1-2 (←)	SW1-1 (→)
R	R	R	R	R	R	R	R

This register stores the bit pattern of the application switch (SW1 to SW3) key input status.

(1) SWn

SWn bit	Setting
0	Application switch key input: OFF (Initial value)
1	Application switch key input: ON

6.5.7 Key Input Status Register (KEYSR)

Address: 0x0062 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	PONSWF	ARKEYF	KEY_OFFF	KEY_ONF	0
R	R	R	R/W	R/W	R/W	R/W	R

(1) KEY_ONF

KEY_ONF bit	Setting
0	An application switch key has not been turned on (Initial value)
1	An application switch key has been turned on. At this time, if the KEY_ONI bit is set to ''1,'' a key ON interrupt occurs. [Clear condition] "0'' is written with the KEY_ONF bit set to ''1.''

(2) KEY_OFFF

KEY_OFFF bit	Setting
0	An application switch key is ON or OFF. (Initial value)
1	An application switch key has changed from ON to OFF. (Initial value) At time, if the KEY_OFFI bit is set to "1,'' a key OFF interrupt occurs. [Clear condition] "0'' is written with the KEY_OFFI bit set to ''1.''

(3) ARKEYF

ARKEYF bit	Setting
0	The same application switch key is not ON for the time specified in the key auto repeat time register (Initial value)
1	The same application switch key is not ON for the time specified in the key auto repeat time register. At this time, if the ARKEYI bit is set to ''1,'' repeat interrupt occurs. [Clear condition] ''0'' is written with the ARKEYF bit set to "1.''

(4) PONSWF

PONSWF bit	Setting
0	The power-on switch has not been turned on for 2sec or more.
1	itch has been turned on for 2 sec or more. At this time, if the PONSWI bit is set to "1," a power-on interrupt occurs.] "0" is written to the PONSWF bit set to "1."

[Supplementary description on application switch key input]

(1) When multiple keys are pressed at the same time, the corresponding bits are all set to “1,” and a KEY_ONF interrupt occurs so long as it is enabled.

(2) If data in the key bit pattern register changes when multiple keys are pressed at the same time, a KEY_ONF interrupt occurs so long as it is enabled.

- Example -

This KEY_ONF interrupt occurs when the state with switches SW1 and SW2 pressed simultaneously changes to one with switches SW1 and SW3 pressed simultaneously.

(3) When multiple keys are released in the state with the keys pressed and held, a KEY_OFFI interrupt occurs so long as it is enabled.

(4) When multiple keys are released, the key states immediately before key release are retained in the key bit pattern register.

6.5.8 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for key input.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) KEYIF

KEYIF bit	Setting
0	The PONSWF, ARKEYF, KEY_OFFF, and KEY_ONF bits of the key input status register are all set to "0." (Initial value)
1	One of the PONSWF, ARKEYF, KEY_OFFF, or KEY_ONF bits of the key input status register is set to "1." "0" is written with the KEYIF bit set to "1."

6.6 Power Supply Control

This section describes the power supply control functions. Table 6.6 summarizes the power supply control registers. In addition, refer to 6.6.1 to 6.6.3 for details of each register.

(1) T-Engine is turned ON or OFF.

(2) When T-Engine is OFF, it is turned ON if the power-on switch is pressed for 2 seconds or more.

(3) T-Engine can be turned OFF from the SH7760.

(4) If the DIP switch (SW7) is set to ON, T-Engine is also turned ON at the same time the power supply controller is turned ON.

Table 6.6 Power Control Registers

Register	Abbreviation	Address	R/W	Size	Remarks
System power control register 1	SPOWCR1	0x0070	R/W	1 byte	
System power control register 2	SPOWCR2	0x0071	R/W	1 byte	

6.6.1 System Power Control Register 1 (SPOWCR1)

Address: 0x0070 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPOWER
R	R	R	R	R	R	R	R/W

(1) SPOWER

SPOWER bit	Setting
0	System power supply: OFF
1	System power supply: ON (Initial value)

6.6.2 System Power Control Register 2 (SPOWCR2)

Address: 0x0071 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SFPOWER
R	R	R	R	R	R	R	R/W

(2) SFPOWER

SFPOWER	Setting
0	T-Engine is turned OFF by SH7760 control.
1	T-Engine is turned OFF by pressing the power-on switch. (Initial value)

6.6.3 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for power control.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) POWERIF

This bit will be functionally enhanced in the future. Don’t access this register. When read, this bit is always 0.”

6.7 LCD Front Light Control

This section describes the LCD light control functions. In addition, Table 6.7 summarizes the front light control registers.

(1) Controlling the ON/OFF state of the LCD front light

Table 6.7 LCD front light register

Register	Abbreviation	Address	R/W	Size	Remarks
LCD front light register	LCDR	0x00A1	R/W	1 byte	

6.7.1 LCD Front Light Register (LCDR)

Address: 0x00A1 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	FRONTL
R	R	R	R	R	R	R	R/W

(1) FRONTL

FRONTL bit	Setting
0	The LCD front light is turned ON.
1	The LCD front light is turned OFF. (Initial value)

6.8 Reset Control

This section describes the reset control functions. Table 6.9 summarizes the reset control registers.

(1) T-Engine reset is controlled.

Table 6.9 Reset Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Reset control register	RESTCR	0x00A2	R/W	1byte	

6.8.1 RESTCR Register (RESTCR)

Address: 0x00A2 Initial value: 0x02

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SWRES	SORES
R	R	R	R	R	R	R/W	R/W

(1) SORES

SORES bit	Setting
0	T-Engine is not restarted by reset. (Initial value)
1	T-Engine is restarted by reset.

If this bit is set to “1,” T-Engine is restarted.

(2) SWRES

SWRES bit	Setting
0	Devices other than the power supply controller are reset with the reset switch (SW2).
1	All the devices covering the power supply controller are reset with the reset switch (SW2). (Initial value)

6.9 Infrared Remote Control

This section describes the infrared remote control functions. Table 6.9 summarizes the infrared remote control functions. For details of each register, refer to 6.9.1 to 6.9.8.

(1) Support of formats for two kinds of infrared remote control signal

- Supported format: NEC format and Home Appliance Manufacturer's Association format

(2) Function for receiving infrared remote control signals

- A maximum of 255 bytes of the infrared remote control signal can be stored. Receive data can be read from the receiving FIFO data register (IRRRFDR).
- Infrared remote control signals of a specified format can be received.
- When a frame signal has been received, a receiving interrupt may be generated.

(3) Function for transmitting infrared remote control signals

- A maximum of 255 bytes of the infrared remote control signal can be transmitted.
- Transmit data can be written to the transmitting FIFO data register (IRRSFDR).
- Infrared remote control signals of the specified format are transmitted.

Table 6.9 Infrared Remote Control Registers

Register	Abbreviation	Address	R/W	Size
Infrared remote control register	IRRCR	0x00B0	R/W	1 byte
Infrared remote status register	IRRSR	0x00B1	R/W	1 byte
Receive data count register for infrared remote control signals	IRRRDNR	0x00B2	R	1 byte
Transmit data count register for infrared remote control signals	IRRSDNR	0x00B3	R	1 byte
Receive FIFO data register for infrared remote control signals	IRRRFDR	0x00B4	R	1 byte
Transmit FIFO data register for infrared remote control signals	IRRSFDR	0x00B5	W	1 byte

6.9.1 Infrared Remote Control Register (IRRCR)

Address; 0x00B0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TDIE	RDIE	FORMAT	START
R	R	R	R	R/W	R/W	R/W	R/W

(1) START

START bit	Setting
0	control is disabled. (Initial value)
1	Infrared remote control is enabled to start data transmission/reception.

(2) FORMAT

FORMAT bit	Setting
0	The NEC format is set. (Initial value)
1	The Home Appliance Manufacturer's Association format is set.

(3) RDIE

RDIE bit	Setting
0	An interrupt is disabled upon completion of receiving a frame of infrared remote control signal. (Initial value)
1	An interrupt is enabled upon completion of receiving a frame of infrared remote control signal.

(4) TDIE

TDIE bit	Setting
0	An interrupt is disabled upon completion of transmitting a frame of infrared remote control signal. (Initial value)
1	An interrupt is enabled upon completion of transmitting a fame of infrared remote control signal.

6.9.2 Infrared Remote Control Status Register (IRRSR)

Address: 0x00B1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TDI	RDI	0	RDBFER
R	R	R	R	R/W	R/W	R	R/W

(1) RDBFER

RDBFER bit	Setting
0	A buffer full error has not occurred during a receive operation. (Initial value)
1	A buffer full error has occurred during a receive operation.

(2) RDI

RDI bit	Setting
0	A frame of data has not been received. (Initial value)
1	A frame of data has been received. [Clear condition] "0" is written with the RDI bit set to "1."

(3) TDI

TDI bit	Setting
0	A frame of data has not been transmitted. (Initial value)
1	A frame of data has been transmitted. [Clear condition] "0" is written with the TDI bit set to "1."

6.9.3 Receive Data Count Register for Infrared Remote Control Signals (IRRRDNR)

Address: 0x00B2 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRRD_D7	IRRRD_D6	IRRRD_D5	IRRRD_D4	IRRRD_D3	IRRRD_D2	IRRRD_D1	IRRRD_D0
R	R	R	R	R	R	R	R

This register indicates the number of received data items (infrared remote control signals) stored in the receive FIFO register. When this register is "0x00," it indicates that there is no data. When the value of this register is "0xFF," it indicates that the receive FIFO register is full of data.

6.9.4 Transmit Data Count Register for Infrared Remote Control Signals (IRRSDNR)

Address: 0x00B3 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRSD_D7	IRRSD_D6	IRRSD_D5	IRRSD_D4	IRRSD_D3	IRRSD_D2	IRRSD_D1	IRRSD_D0
R	R	R	R	R	R	R	R

This register indicates the number of data items not transmitted (infrared remote control signals) stored in the transmit FIFO register. When the value of this register is “0x00,” it indicates that there is no data. When the value of this register is “0xFF,” it indicates that the transmit FIFO buffer is full of data.

6.9.5 Receive FIFO Data Register for Infrared Remote Control Signals (IRRRFDR)

Address: 0x00B4 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRRDR_D7	IRRRDR_D6	IRRRDR_D5	IRRRDR_D4	IRRRDR_D3	IRRRDR_D2	IRRRDR_D1	IRRRDR_D0
R	R	R	R	R	R	R	R

This register is an 8-bit FIFO register for storing received data. All the received data can be obtained from this register until it is emptied. For details, refer to 6.9.8, “Infrared Remote Control Data Structure.”

6.9.6 Transmit FIFO Data Register for Infrared Remote Control Signals (IRRSFDR)

Address: 0x00B5 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRSDR_D7	IRRSDR_D6	IRRSDR_D5	IRRSDR_D4	IRRSDR_D3	IRRSDR_D2	IRRSDR_D1	IRRSDR_D0
W	W	W	W	W	W	W	W

This register is an 8-bit FIFO register that stores transmission data. Transmission data can be stored until this register is filled with data. For details, refer to 6.9.8, “Infrared Remote Control Data Structure.”

6.9.7 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for infrared remote control signals.

Address: 0x0090 Initial value: 0x00

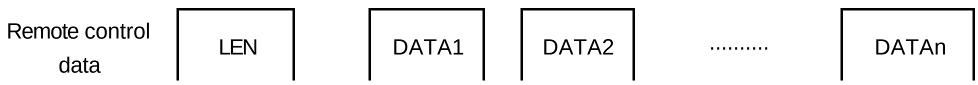
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) IRRIF

IRRIF bit	Setting
0	A frame of data has not been transmitted or received. (Initial value)
1	A frame of data has been transmitted or received. [Clear condition] "0" is written with the IRRIF bit set to "1."

6.9.8 Infrared Remote Control Data Structure

The following shows the relation between the infrared remote control data and repeat codes. In addition, it



shows a structure of remote control data in the NEC format.

Example) NEC format remote control data



[Infrared Remote Control Operation Procedure]

[Initial setting]

(1) Two kinds of formats are set by selecting the FORMAT bit of the IRRCR register.
(2) The START bit of the IRRCR register is set to "1" to start infrared remote control and infrared signal reception
(3) To enable an interrupt at the time of receiving a frame of the signal, the RDIE bit is set to "1."
(4) To enable an interrupt at the time of transmitting a frame of the signal, the TDIE bit is set to "1."

[For infrared signal reception]

(1) When a frame of data has been received (RDI=1), the IRRIF bit of the RTKISR register is set to "1."
(2) When an interrupt at completion of signal reception has been enabled (RDIE=1), an interrupt occurs when a frame of data is stored in the IRRRFDE register.
(3) To obtain the received data, the receiving FIFO data register (IRRRFDR) is read. The IRRRFDR register contains a data count (that indicates the number of items of one frame of data received) and the received data itself. If this register is read, the data count and data itself are output in this order.
(4) The size of received data is set in the received data count register (IRRRDNR). When two frames have been received, the total data count and the two frames of data are set in the received data count register (IRRRDNR).

[For infrared signal transmission]

(1) When transmission data is transmitted, it is written to the transmitting FIFO data register. The data count for one frame of transmission data and the data itself are written to this data register. In addition, this transmission data count is not counted as transmission data.
(2) The count for data not transmitted is set in the transmission data count register (IRRSDNR).
(3) Data can be written to the transmission data IRRSFDR until the count for data not transmitted (IRRSDNR) reaches 255.
(4) When a frame of data has been transmitted (TDI=1), the IRRIF bit of the RTKISR register is set to "1." An interrupt for transmission completion occurs so long as it is enabled.

⚠ CAUTION

- To change the type of format, the FORMAT value of the same register must be set before the START bit of the IRRCR register is set to "1."
- When the START bit of the IRRCR register is "0," transmission/reception is not guaranteed.
- When the specified size is larger than the IRRRDNR value during a read operation, "FF" is set for excessive read data.
- Only the custom code and data code are specified for transmission data, and the leader, stop bit, frame space, and trailer are automatically added.
- When the number of write data items is larger than that of the remaining transmission data (255–byte transmission data count register IRRSDNR), a data length error occurs.
- When the IRRRFDR register has become full during a read operation, the buffer full error bit is set to "1," and the data received later is discarded.
- The IRRIF bit of the RTKISR register is cleared when "0" is written with the IRRIF bit set to "1."

6.10 Serial EEPROM Control

This section describes the EEPROM control functions. Table 6.10 summarizes the serial EEPROM control registers. For details of each register, refer to 6.10.1 to 6.10.3.

(1) Serial EEPROM (512 bytes) can be read and written.

Table 6.10 Serial EEPROM Control Registers

Register	Abbreviation	Address	R/W	Size
EEPROM control register	EEPCR	0x00C0	R/W	1 byte
EEPROM data register	EEPDR	0x0100~0x02FF	R/W	1 byte x 512

6.10.1 EEPROM Control Register (EEPCR)

Address: 0x00C0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	START
R	R	R	R	R	R	R	R/W

(1) START

START bit	Setting
0	The serial EEPROM is disabled. (Initial value)
1	ROM is enabled.

6.10.2 EEPROM Data Register (EEPDR)

Address: 0x0100 to 0x02FF Initial value: Not defined

D7	D6	D5	D4	D3	D2	D1	D0
EEPDR_D7	EEPDR_D6	EEPDR_D5	EEPDR_D4	EEPDR_D3	EEPDR_D2	EEPDR_D1	EEPDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register consists of 512 8-bit data in the above format.

EEPDR address	
0x0100	8 bit
0x0101	8 bit
	- - -
0x02FE	8 bit
0x02FF	8 bit

An EEPROM address corresponds to an EEPDR address. When a read/write operation is performed on the EEPROM, the EEPDR address must be specified for the operation.

6.10.3 Serial EEPROM Operation Procedure

[Initial Setting]

(1) The START bit of the EEPCR register is set to “1.”

[For a read/write operation to the serial EEPROM]

(1) An EEPDR address corresponding to an EEPROM address must be specified for a read/write operation.

⚠ CAUTION
When the START bit of the EEPCR register is “0,” read/write data is not guaranteed.

6.11 Electronic Volume Control

This section describes the electronic volume control functions. Table 6.11 summarizes the electronic volume control registers. For details of each register, refer to 6.11.1 and 6.11.2.

(1) An electronic volume value can be set.

An electronic volume value can be set within a range from 0x00 (minimum sound volume) to 0xFF (maximum sound volume).

(2) Two electronic volume values can be set.

An electronic volume value can be set for the right or left speaker.

Table 6.11 Electronic Volume Control Registers

Register	Abbreviation	Address	R/W	Size
Electronic volume data register for the right speaker	EVRDR	0x00D0	R/W	1 byte
Electronic volume data resister for the left speaker	EVLDR	0x00D1	R/W	1 byte

6.11.1 Electronic Volume Data Register for the Right Speaker (EVRDR)

Address: 0x00D0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EVRDR_D7	EVRDR_D6	EVRDR_D5	EVRDR_D4	EVRDR_D3	EVRDR_D2	EVRDR_D1	EVRDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Values from 0x00 to 0xFF can be set.

6.11.2 Electronic Volume Data Register for the Left Speaker (EVLDR)

Address: 0x00D1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EVLRD_D7	EVLRD_D6	EVLDR_D5	EVLDR_D4	EVLDR_D3	EVLDR_D2	EVLDR_D1	EVLDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Values from 0x00 to 0xFF can be set.

6.12 Power Supply Controller Initial Values

The register values for the power supply controller vary depending on the following conditions. Under condition A, all the power supply controller registers are initialized. The initial value of each register is given in the description of each register in this manual.

For register values under conditions A to D, refer to the following table of RTC registers.

[Condition]

Condition A: The power is turned ON.
The hard reset switch (SW4) is pressed.

Condition B: The power is turned ON.
The RESTCR SORES bit has been set to "1."
The RESTCR SWRES bit has been set to "1," and the reset switch (SW2) has been pressed.

Condition C The RESTCR SWES bit has been cleared to zero and the reset switch (SW2) has been pressed.

Condition D: The SPOWCR1 SPOWER bit has been set to "0."

Table 6.12 Values under RTC Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
RTC control register	RTCCR	Initial value	Initial value	Hold	Initial value
RTC status register	RTCSR	Initial value	Hold	Hold	Hold
Second counter	SECCNT	Initial value	Operation	Operation	Operation
Minute counter	MINCNT	Initial value	Operation	Operation	Operation
Hour counter	HRCNT	Initial value	Operation	Operation	Operation
Day-of-the-week counter	WKCNT	Initial value	Operation	Operation	Operation
Day counter	DAYCNT	Initial value	Operation	Operation	Operation
Month counter	MONCNT	Initial value	Operation	Operation	Operation
Year counter	YRCNT	Initial value	Operation	Operation	Operation
Second alarm counter	SECAR	Initial value	Hold	Hold	Hold
Minute alarm counter	MINAR	Initial value	Hold	Hold	Hold
Hour alarm counter	HRAR	Initial value	Hold	Hold	Hold
Day-of-the-week alarm counter	WKAR	Initial value	Hold	Hold	Hold
Day alarm counter	DAYAR	Initial value	Hold	Hold	Hold
Month alarm counter	MONAR	Initial value	Hold	Hold	Hold
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Figure 6.13 Values under Touch Panel Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Touch panel control register	TPLCR	Initial value	Initial value	Hold	Initial value
Touch panel status register	TPLSR	Initial value	Initial value	Hold	Initial value
Touch panel sampling control register	TPLSCR	Initial value	Initial value	Hold	Initial value
X position A/D register	XPAR	Initial value	Initial value	Hold	Initial value
Y position A/D register	YPAR	Initial value	Initial value	Hold	Initial value
X position dot register	XPDR	Initial value	Initial value	Hold	Initial value
Y position dot register	YPDR	Initial value	Initial value	Hold	Initial value
XA position dot register	XAPDR	Initial value	Hold	Hold	Hold
YA position dot register	YAPDR	Initial value	Hold	Hold	Hold
XB position dot register	XBPDR	Initial value	Hold	Hold	Hold
YB position dot register	YBPDR	Initial value	Hold	Hold	Hold
XC position dot register	XCPDR	Initial value	Hold	Hold	Hold
YC position dot register	YCPDR	Initial value	Hold	Hold	Hold
XA position A/D register	XAPAR	Initial value	Hold	Hold	Hold
YA position A/D register	YAPAR	Initial value	Hold	Hold	Hold
XB position A/D register	XBPAR	Initial value	Hold	Hold	Hold
YB position A/D register	YBPAR	Initial value	Hold	Hold	Hold
XC position A/D register	XCPAR	Initial value	Hold	Hold	Hold
YC position A/D register	YCPAR	Initial value	Hold	Hold	Hold
DX dot register	DXDR	Initial value	Hold	Hold	Hold
DY dot register	DYDR	Initial value	Hold	Hold	Hold
X position dot calculation A/D value	XPARDOT	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 1	XPARDOT1	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 2	XPARDOT2	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 3	XPARDOT3	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 4	XPARDOT4	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value	YPARDOT	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 1	YPARDOT1	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 2	YPARDOT2	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 3	YPARDOT3	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 4	YPARDOT4	Initial value	Hold	Hold	Hold
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.14 Values under Switch Input Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Key control register	KEYCR	Initial value	Initial value	Hold	Initial value
Key auto repeat time register	KATIMER	Initial value	Initial value	Hold	Initial value
Key input status register	KEYSR	Initial value	Initial value	Hold	Initial value
Key bit pattern register	KBITPR	Initial value	Initial value	Hold	Initial value
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.15 Values under Power Supply Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
System power control register 1	SPOWCR1	Initial value	Initial value	Hold	0x00
System power snort register 2	SPOWCR2	Initial value	Initial value	Hold	Initial value
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.16 Values under LED Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
LED register	LEDR	Initial value	Initial value	Hold	0x00

Table 6.17 Values under LCD Front Light Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
LCD front light register	LCDR	Initial value	Initial value	Hold	0x00

Table 6.18 Values under Reset Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Reset control register	RESTCR	Initial value	Initial value	Hold	Initial value

Table 6.19 Values under Infrared Remote Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Infrared remote control register	IRRCR	Initial value	Initial value	Hold	Initial value
Infrared remote control status register	IRRSR	Initial value	Initial value	Hold	Initial value
Receive data count register for infrared remote control signals	IRRRDNR	Initial value	Initial value	Hold	Initial value
Transmit data count register for infrared remote control signals	IRRSDNR	Initial value	Initial value	Hold	Initial value
Receiving FIFO data register for infrared remote control signals	IRRRFDR	Initial value	Initial value	Hold	Initial value
Transmitting FIFO data register for infrared remote control signals	IRRSFDR	Initial value	Initial value	Hold	Initial value

Table 6.20 Values under Serial EEPROM Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
EEPROM control register	EEPCR	Initial value	Initial value	Hold	Initial value
EEPROM data register	EEPDR	Initial value	Initial value	Hold	Initial value

Table 6.21 Values under Electronic Volume Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Electronic volume data register for the right speaker	EVRDR	Initial value	Initial value	Hold	Initial value
Electronic volume data register from the left speaker	EVLDR	Initial value	Initial value	Hold	Initial value

7. External Interrupts

7.1 SH7760 External Interrupts

Figure 7.1 shows a mechanism for the SH7760 interrupt signal.

Table 7.1 shows the levels for respective interrupt signals.

As shown in Figure 7.1, interrupt signals from devices within T-Engine are sent to the pins /IRQ4, PINT11, PINT6 and PINT7 of theSH7760. The interrupt signals /IRQ0 to /IRQ3 are converted into the /IRL signals by FPGA, then output to the /IRL [3:0] of the SH7760.

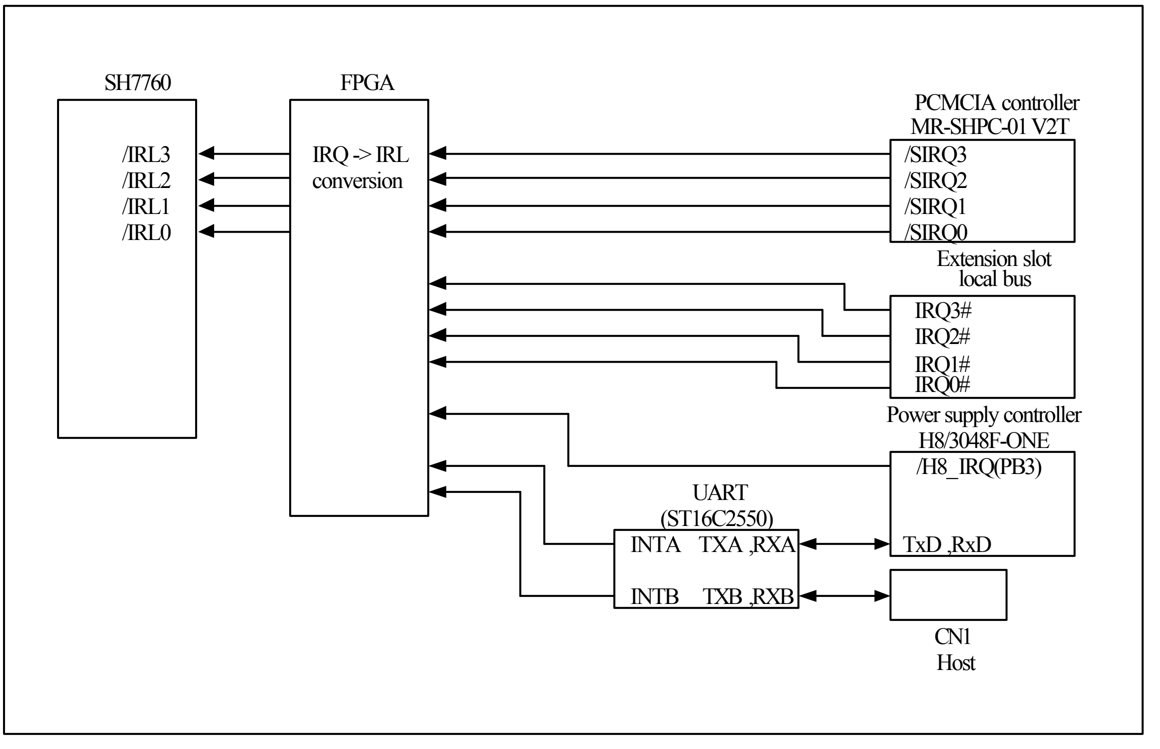


Figure 7.1 Interrupt Signal Mechanism

Table 7.1 Interrupt Levels for Interrupt Signals

No.	Interrupt request source	Interrupt input pin	Interrupt signal level	Remarks
1	PCMCIAcontroller (SIRQ3)	/IRL [3:0]	/IRL [3:0] = 0001	Interrupt level 14
2	PCMCIAcontroller (SIRQ2)	/IRL [3:0]	/IRL [3:0] = 0101	Interrupt level 10
3	PCMCIAcontroller (SIRQ1)	/IRL [3:0]	/IRL [3:0] = 1000	Interrupt level 7
4	PCMCIAcontroller (SIRQ0)	/IRL [3:0]	/IRL [3:0] = 1010	Interrupt level 5
5	UART controller chA	/IRL [3:0]	/IRL [3:0] = 0110	Interrupt level 9
6	UART controller chB	/IRL [3:0]	/IRL [3:0] = 0011	Interrupt level 12
7	H8/3048F-ONE	/IRL [3:0]	/IRL [3:0] = 0010	Interrupt level 13
8	Extension slot (IRQ3#)	/IRL [3:0]	/IRL [3:0] = 0000	Interrupt level 15
9	Extension slot (IRQ2#)	/IRL [3:0]	/IRL [3:0] = 0100	Interrupt level 11
10	Extension slot (IRQ1#)	/IRL [3:0]	/IRL [3:0] = 0111	Interrupt level 8
11	Extension slot (IRQ0#)	/IRL [3:0]	/IRL [3:0] = 1001	Interrupt level 6

8. T-Engine Extension Slot

8.1 Extension Slot Specifications

Connector number: CN2

T-Engine connector model: 20-5603-14-0101-861 (Kyocera Elco)

Adaptable connector model: 10-5603-14-0101-861 (Kyocera Elco)

Figure 8.1 shows the location of an extension slot.

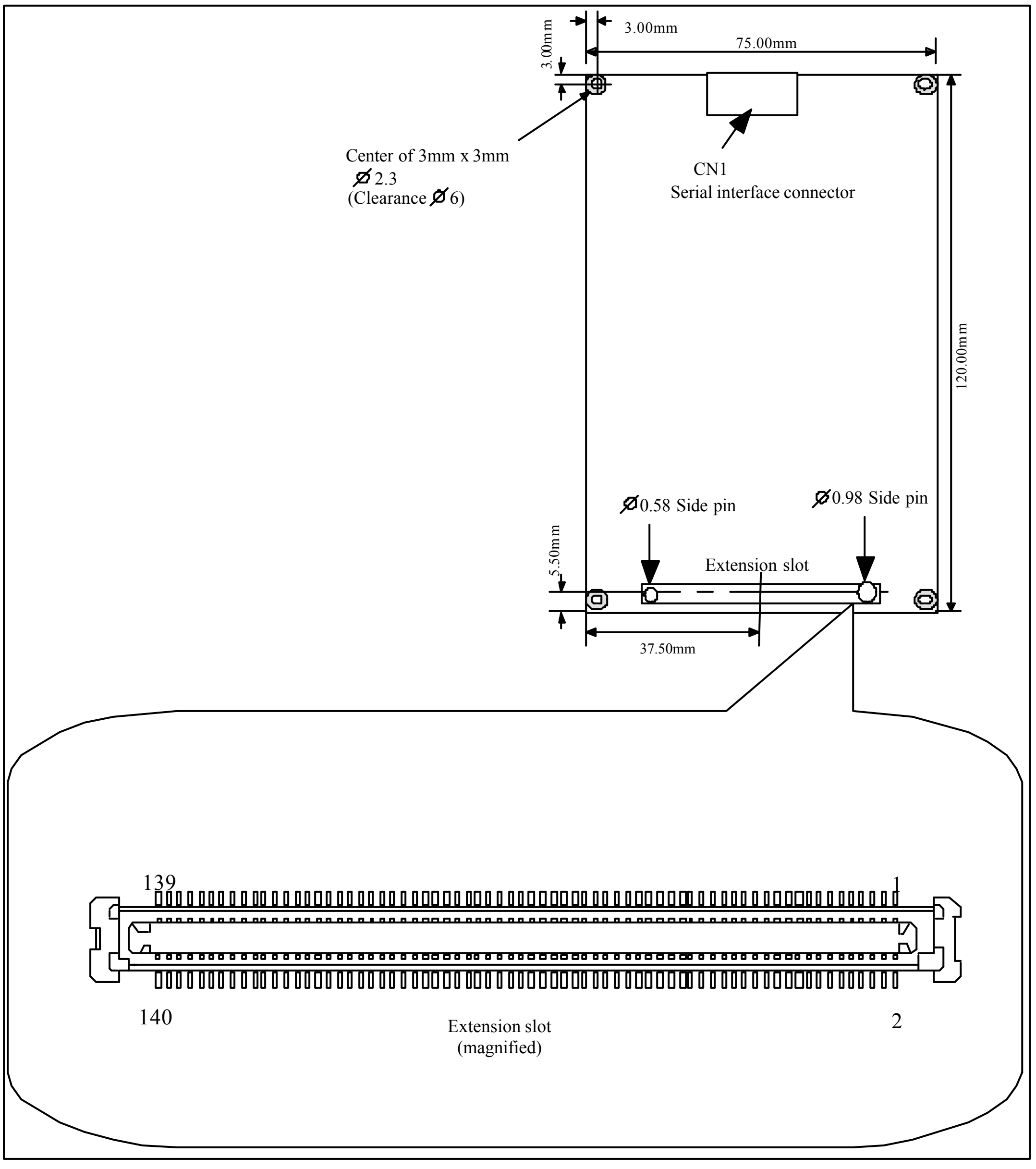


Figure 8.1 Extension Slot Position

8.2 Extension Slot Signal Assignment

Table 8.1 shows the assignment of extension slot signals.

Table 8.1 Extension Slot Signals

Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O
1	5V (*1)	-	36	D29	I/O	71	A24	OUT	106	SCIF2_CTS#	IN
2	5V	-	37	D30	I/O	72	A25	OUT	107	-	-
3	5V	-	38	D31	I/O	73	EPROMCE#	OUT	108	-	-
4	5V	-	39	GND	-	74	CS2#	OUT	109	GND	-
5	D0	I/O	40	GND	-	75	CS4#	OUT	110	GND	-
6	D1	I/O	41	CKIO	OUT	76	CS5#	OUT	111	TCK	IN
7	D2	I/O	42	GND	-	77	RDWR	OUT	112	TMS	IN
8	D3	I/O	43	GND	-	78	BS#	OUT	113	TRST#	IN
9	D4	I/O	44	GND	-	79	GND	-	114	TDI	IN
10	D5	I/O	45	A0	OUT	80	GND	-	115	TDO	OUT
11	D6	I/O	46	A1	OUT	81	RD#	OUT	116	ASEBRKAK#	OUT
12	D7	I/O	47	A2	OUT	82	WAIT#	IN	117	3.3VSB (*3)	-
13	D8	I/O	48	A3	OUT	83	WE0#	OUT	118	3.3VSB	-
14	D9	I/O	49	A4	OUT	84	WE1#	OUT	119	3.3VSB	-
15	D10	I/O	50	A5	OUT	85	WE2#	OUT	120	3.3VSB	-
16	D11	I/O	51	A6	OUT	86	WE3#	OUT	121	AUDATA0	I/O
17	D12	I/O	52	A7	OUT	87	GND	-	122	AUDATA1	I/O
18	D13	I/O	53	A8	OUT	88	GND	-	123	AUDATA2	I/O
19	D14	I/O	54	A9	OUT	89	IRQ0#	IN	124	AUDATA3	I/O
20	D15	I/O	55	A10	OUT	90	IRQ1#	IN	125	AUDSYNC#	OUT
21	GND	-	56	A11	OUT	91	IRQ2#	IN	126	AUDCK	IN
22	GND	-	57	A12	OUT	92	IRQ3#	IN	127	3.3V (*4)	-
23	D16	I/O	58	A13	OUT	93	NMI_IN	IN	128	3.3V	-
24	D17	I/O	59	A14	OUT	94	RST_IN#	IN	129	3.3V	-
25	D18	I/O	60	A15	OUT	95	RST_OUT#	OUT	130	3.3V	-
26	D19	I/O	61	GND	-	96	DREQ#	IN	131	3.3V	-
27	D20	I/O	62	GND	-	97	DRAK#	OUT	132	3.3V	-
28	D21	I/O	63	A16	OUT	98	DACK#	OUT	133	VBAT_IN (*5)	-
29	D22	I/O	64	A17	OUT	99	ROMSEL	IN	134	VBAT_IN	-
30	D23	I/O	65	A18	OUT	100	BASE# (*2)	IN	135	VBAT_IN	-
31	D24	I/O	66	A19	OUT	101	GND	-	136	VBAT_IN	-
32	D25	I/O	67	A20	OUT	102	GND	-	137	GND	-
33	D26	I/O	68	A21	OUT	103	SCIF2_TXD	OUT	138	GND	-
34	D27	I/O	69	A22	OUT	104	SCIF2_RXD	IN	139	GND	-
35	D28	I/O	70	A23	OUT	105	SCIF2_RTS#	OUT	140	GND	-

(shaded box) : Indicates the address bus, data bus, control signals, and serial signals of the SH7760. Supply voltage is 3.3V.

*1: 5.0V (typ.) is supplied when the SH7760 is turned on.

*2: If this pin is set to "Low," output takes place from the SH7760 extension to the extension slot.

*3: 3.3V (typ.) is supplied when the battery is provided or the AC adapter is connected.

*4: 3.3V (typ.) is supplied when the SH7760 is turned on.

*5: Pin for power supply (4.2V to 3.6V). T-Engine can be powered via the extension slot.

9. Daughter Board Design Guide

This chapter describes the design of the daughter board to be connected to the extension slot of T-Engine. The daughter board may contain user-specific devices and can be controlled by the address bus, data bus, and control signals or serial signals (start-stop) of the SH7760 that connect to the extension slots of T-Engine.

9.1 Daughter Board Dimensions

The recommended daughter board size is the CPU board size (120mm x 75mm) of T-Engine.

9.2 Daughter Board Power Supply

Table 9.1 shows the voltage and current that can be supplied from T-Engine to a daughter board. When a daughter board requires more current, a power supply must be mounted on the daughter board.

Table 9.1 Voltage and Current to the Daughter Board

Extension slot signal name	Output voltage	Permissible current	Remarks
3.3V 3.3VSB	3.3V	250mA	3.3V: Supplied when the SH7760 is turned ON. 3.3VSB: Always supplied when the AC adapter is connected.
5V	5V	250mA	Supplied when the SH7760 is turned ON.

⚠ CAUTION

When a peripheral device operating on the bus power via the USB has been connected to T-Engine or the PCMCIA card is in use, the permissible current is the current obtained by subtracting the dissipation current of the device and card from the permissible current.

9.3 Daughter Board Stack

A maximum of 3 daughter boards can be stacked. When multiple daughter boards are stacked, care should be taken for electric capacity. Figure 9.2 shows an example of daughter board stacks.

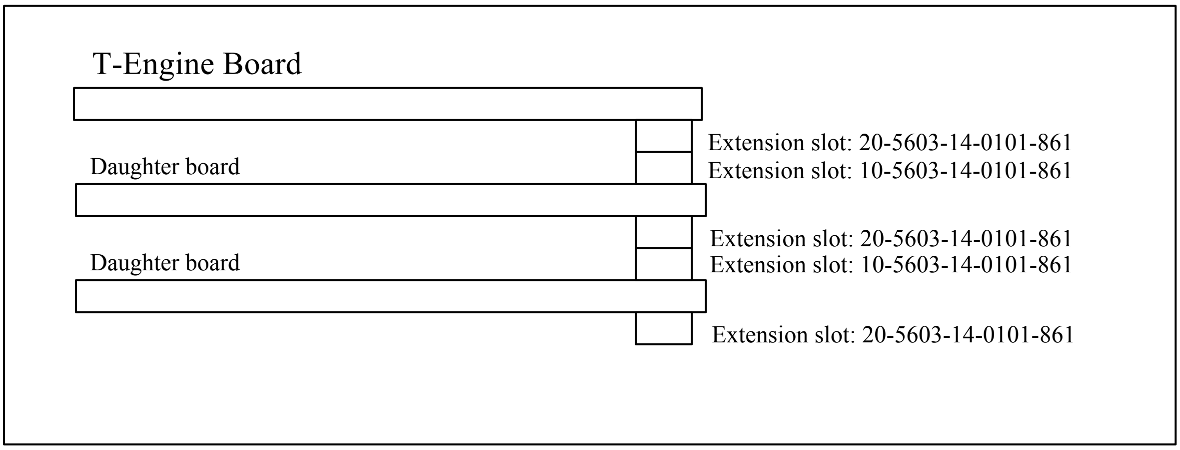


Figure 9.2 Daughter Board Stack

9.4 Daughter Board WAIT# Output

T-Engine is provided with a WAIT# input pin on the extension slot for WAIT input to the daughter board. When a WAIT# is output from the daughter board, open collector output must take place to prevent a collision of WAIT# output when multiple daughter boards are stacked.

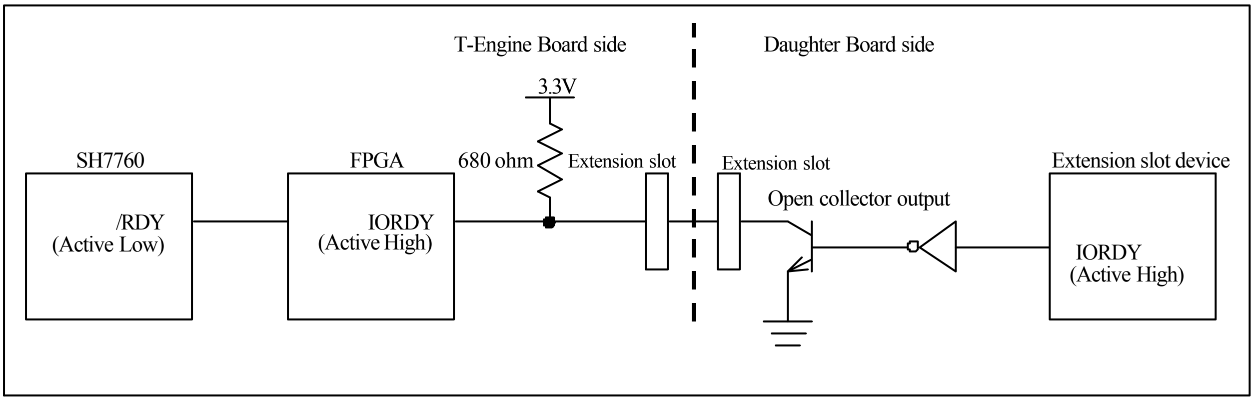


Figure 9.3 Extension Slot IORDY Pin Structure

9.5 Extension Slot AC Timing

As shown in Figure 9.4, the SH7760 bus signal is output to the extension slot via the bus buffer. For this reason, the bus signal delays approx. 8nsec for the AC timing of the SH7760 bus. When designing the daughter board, consider this delay. Figure 9.5 shows the basic bus timing of the SH7760.

For details on SH7760 bus timing, refer to the pertinent SH7760 Hardware Manual.

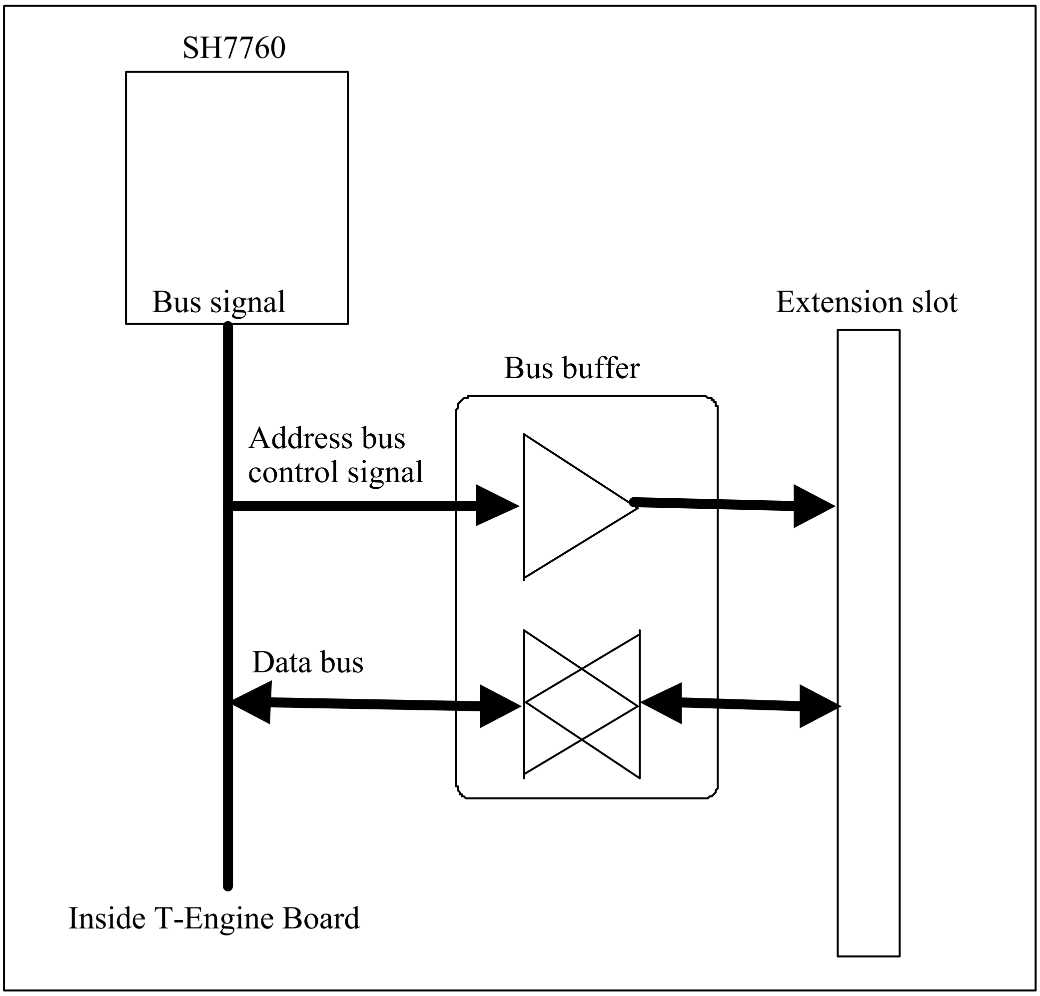


Figure 9.4 Extension Slot Bus Buffer Structure

⚠ CAUTION

The bus timing delay time must be used only for reference. This is not a guaranteed value.

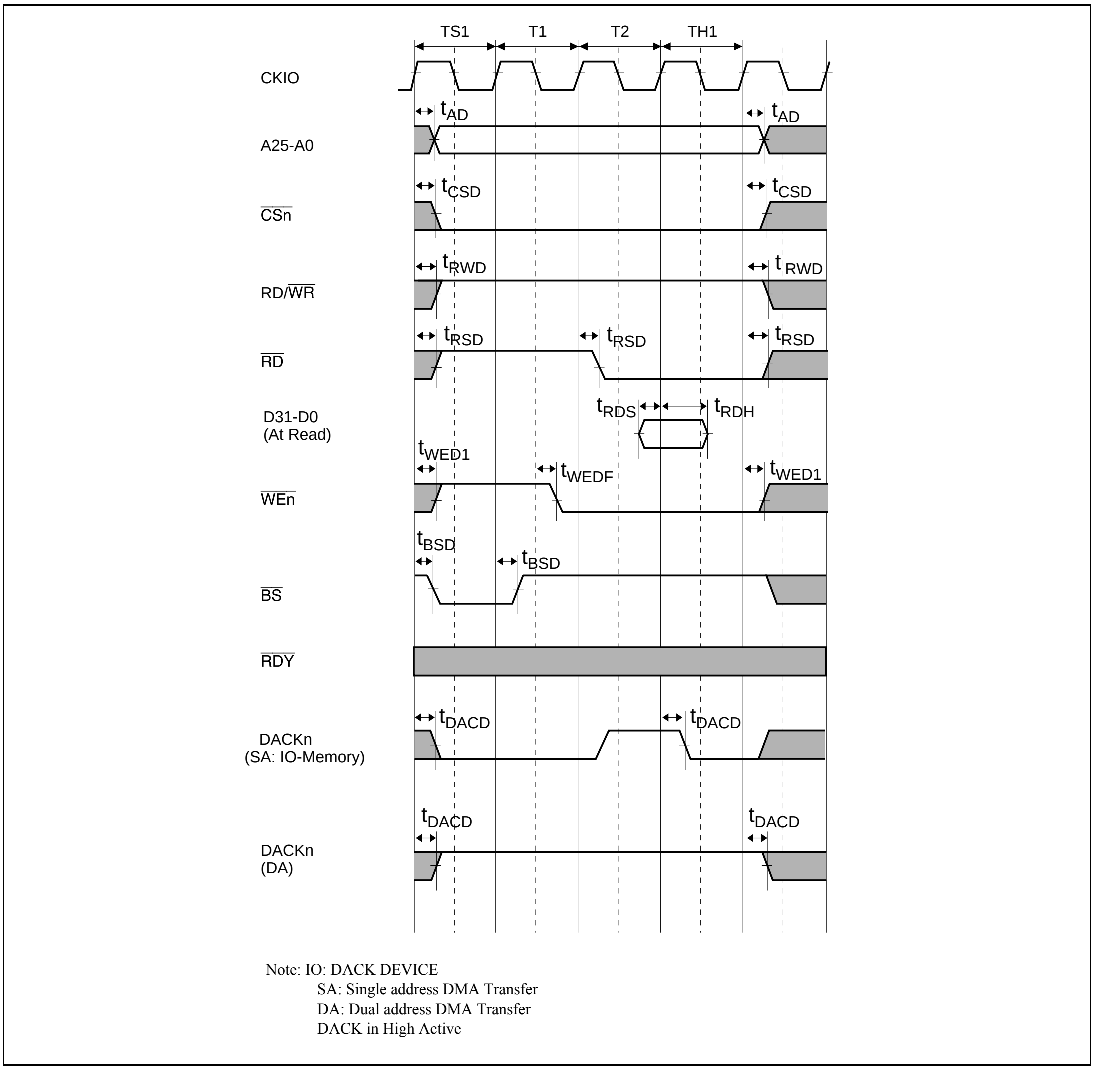


Figure9.5 Memory Byte control SRAM Bus cycle Basic Read cycle
(No wait, Address set up/Insert hold time, AnS=1, AnH=1)

10. Flash Memory Refresh

When refreshing the contents of the flash memory on T-Engine or the internal flash memory of the power supply controller (H8/3048F-ONE), connect the debug board to the extension slot of T-Engine and run the program stored in the EPROM on the debug board.

10.1 Preparation for Flash Memory Refresh

Connect the debug board to the extension slot (CN2) of T-Engine. In addition, make the following settings for the jumper switch.

For details, refer to 2.4.2 "Debug Board Connection" and 2.4.3 "Debug Board Jumper switch."

Debug board jumper switch (J1): Pins 1 and 2 must be short-circuited (EPROM allocation to an address range from h'00000000 to h'001FFFFF).

Connect the serial interface connector (CN1) of T-Engine and host system with an RS-232C interface cable (accessory). Start communication software on the host system and make the following settings.

Baud rate: 115200bps
Data length: 8 bits
Parity bit: None
Stop bit: 1 bit
Flow control: Xon/Xoff

After making the above settings, turn on the power of T-Engine, and the title screen --- screen indicating the execution status of the program stored in the EPROM --- will be displayed on the communication software as shown below.

[Display Screen]

```
==================================================
    SH7760 Self Debugger      Ver  x.xL  (****/**/**)
 -------------------------------------------------------------------------
   (C) Copyright 2002-2005.   Hitachi.Ltd. All rights reserved.
==================================================
   Ready >                                  H [elp] for help messages...
```

10.2 T-Engine Flash Memory

10.2.1 Refresh Method

Figure 10.1 shows how the T-Engine flash memory is refreshed. As shown in Figure 10.1, the T-Engine flash memory is refreshed in such a way that flash memory data is copied to SDRAM and the data transferred from the host system is written to the flash memory.

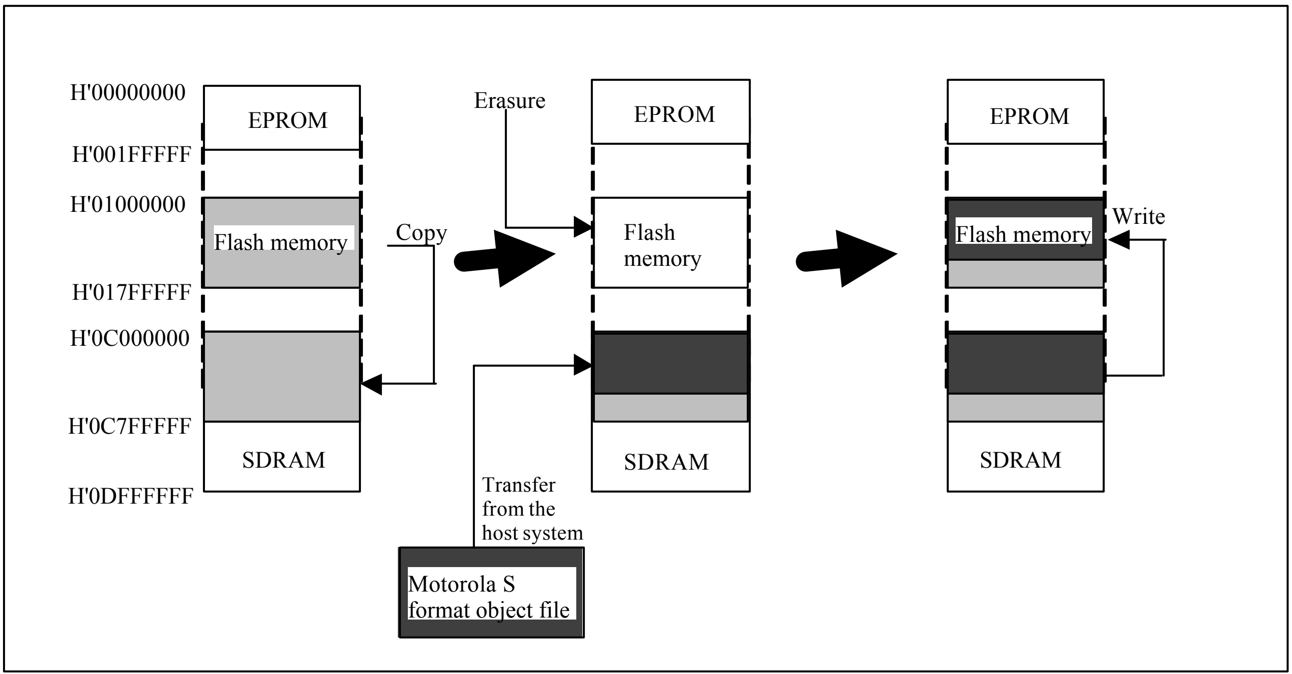


Figure 10.1 Flash Memory Refresh

Below is a description of the T-Engine flash memory refresh method.

(1) As shown on the following screen, type "FL 0" and hit the Enter key after the title screen appears on the communication software.

[Display Screen]

```
Ready >fl 0
```

(2) As shown on the following screen, transfer the Motorola S format object file after the transfer request message "Please Send A S-format Record" appears on the screen.

[Display Screen]

```
SH7760 Flash Memory Change Value!
Flash Memory data copy to RAM
Please Send A S-format Record
```

(3) Flash memory refresh normally terminates when the messages ("flash memory chip erase: complete" and "flash write complete") sequentially appear on the screen after the Motorola S format object file has been transferred.

[Display Screen]

```
Ready >fl 0

SH7760 Flash Memory Change Value!
Flash Memory data copy to RAM
Please Send A S-format Record

Start   Addrs = A0000000
End   Addrs = A00FFFFF

Transfer complete
Flash chip erase: complete
Program :complete
Flash write complete
Ready >
```

10.3 Power Supply Controller’s Internal Flash Memory

10.3.1 Refresh Method

Figure 10.2 shows how the flash memory of the power supply controller is refreshed. As shown in Figure 10.2, data transferred from the host system is saved in the SDRAM when power supply controller’s flash memory is refreshed. The saved data is transferred to the power supply controller and written to the flash memory by the power supply controller firmware. Though the flash memory of the power supply controller has been divided into 8 blocks, the upper 4 blocks are occupied by the firmware for refreshing the flash memory and only the remaining 4 blocks (BLK4 to BLK7) are rewritten.

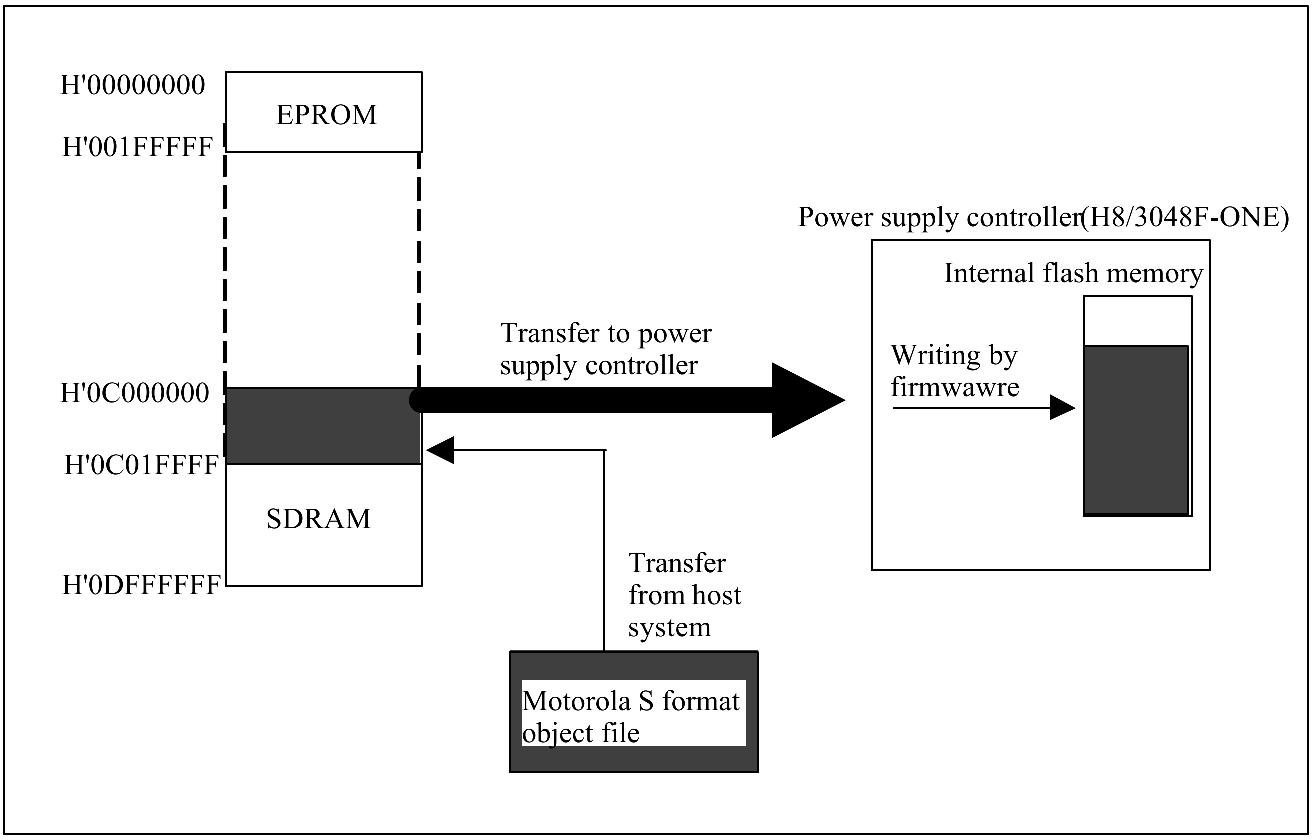


Figure 10.2 Refreshing the Flash Memory of the Power Supply Controller

Below is a description of the method for refreshing the flash memory of the power supply controller.

(1) As shown on the following screen, type "FL 1" and hit the Enter key after the title screen appears on the communication software.

[Display Screen]

```
==================================================
    SH7760 Self Debugger     Ver  x.xL  (****/**/**)
 ------------------------------------------------------------------------------
   (C) Copyright 2002-2005.  Hitachi.Ltd. All rights reserved.
===================================================
   Ready >                                     H [elp] for help messages...
```

Ready>fl 1

(2) As shown on the following screen, transfer the Motorola S format object file after the transfer request message "Please Send A S-format Record" appears on the screen.

Note: After data is transferred, its program ID is checked to determine whether the transferred data is correct. When the program ID is not correct, the message "Wrong Data!!" appears and memory refresh terminates.

[Display Screen]

```
==================================================
    SH7760 Self Debugger     Ver  x.xL  (****/**/**)
 ------------------------------------------------------------------------------
   (C) Copyright 2002-2005.  Hitachi.Ltd. All rights reserved.
===================================================
   Ready >                                     H [elp] for help messages...
```

Ready>fl 1

H8/3048Fone Flash Memory Change Value!

Clear data buffer (all 0xFF)

Please Send A S-format Record

(3) Refreshing the flash memory of the power supply controller normally completes when the messages ("H8 flash erase: complete" and "flash write complete") sequentially appear on the screen after the Motorola S format object file has been transferred.

⚠ CAUTION

When the flash memory of the power supply controller is being refreshed, never power OFF T-Engine. If ignored, refreshing may terminate in error or the flash memory may be damaged.

[Display Screen]

Ready>fl 1

H8/3048Fone Flash Memory Change Value!

Clear data buffer (all 0xFF)

Please Send A S-format Record

Start Addrs = 00001000

End Addrs = 00003D20

Transfer complete

H8 Flash erase: complete

Program :……………. complete

Flash write complete

Ready>

10.3.2 Refresh Check

After the internal flash memory of the power supply controller is refreshed, the version of the refreshed program or the data stored in the internal flash memory of the power supply controller can be checked by entering the following command. However, note that the following command can be executed immediately after the internal flash memory of the power supply controller has been refreshed. When T-Engine has been turned off and on or the reset switch or NMI switch of T-Engine has been pressed, the following command cannot be executed normally.

(1) Reading the version

Enter the command as shown on the following screen, and the version of the written program will be read out. Version information is displayed in X.X.

[Display Screen]

```
Ready>h8_ver
-------------------
ROM Version
-------------------
Hitachi ULSI T-Engine PowerController VerX.X
```

(2) Reading flash memory data

When the command and the address to be read have been entered as shown on the following screen, 64-byte data can be read out from the internal flash memory of the power supply controller.

[Display Screen]

```
Ready>h8d   10000
00010000 : 00 01 02 00 00 01 02 00  00 01 02 00 00 01 02 00
00010010 : 00 01 02 00 00 01 02 00  00 01 02 00 00 01 02 00
00010020 : 00 01 02 00 00 01 02 00  00 01 02 00 00 01 02 00
00010030 : 00 01 04 CC 00 01 05 2A  00 01 02 00 00 01 05 70
```

(3) Restarting the Power Supply Controller

To restart the power supply controller, enter the command as shown on the following screen. Once the power supply controller is restarted, the SH7760 is restarted too.

[Display Screen]

```
Ready>restart
ReStart !!
```

11. Attached Documents

11.1 T-Engine Board Parts List

11.1.1 CPU Board Parts list

CPU Board Parts List (1)

Parts name	Model name	Maker	Quantity	Parts No.
SH7760	HD6417760BP200D	RENESAS	1	U7
H8/3048F-ONE	HD64F3048BVF25	RENESAS	1	U8
PC Card controller	MR-SHPC-01V2T	Marubun	1	U12
UART (2Ch)	ST16C2550CQ48	EXAR	1	U18
AUDIO CODEC	UDA1342TS	PHILIPS	1	U14
ispMACH 4A	M4A3-256/192-7FAC	LATTICE	1	U11
ispMACH 4A	M4A3-32/32-7VC48	LATTICE	1	U10
RTC	RV5C348B	RICOH	1	U17
SWIFT	TPS54316PWP	T.I	1	U16
DC/DC Converter	LTC3440EMS	LTC	1	U15
DC/DC Converter	LTC1772CS6	LTC	1	U1
SIM Level Translator	LTC1555LEGN-1.8	LTC	1	U13
USB power switch	TPS2014D	T.I	1	U23
Digital Potentimeter	MAX5413EUD	MAXIM	1	U26
Power Switch	TPS2211IDB	T.I	1	U20
RS-232 Transceiver	SP3223ECY	SIPEX	1	U2
Headphone amplifier	LM4865MM	NS	2	U27,U28
OP amplifier	NJM2100V<TE1>	JRC	2	U24,U25
u voltage monitor	MAX811REUS-T	MAXIM	1	U22
CBT-LV	SN74CBTLV3383DGV	T.I	1	U4
LV Logic	SN74LV07APW	T.I	1	U21
LV1G Logic	HD74LV1G00ACM<E>	RENESAS	1	U6
LV1G Logic	HD74LV1G08ACM<E>	RENESAS	4	U3,U5,U9,U19
256M SDRAM	HM5225165BTT-A6	ELPIDA	2	M1,M2
64M-Flash Memory	MBM29DL640E90TN	Fujitsu	1	M3
Serial EEPROM	S-29391AFJA	SII	1	M4
LED	SML-310MT<T86>	ROHM	2	LED1,LED2
LED	GL100MN0MP	SHARP	1	LED3
OSC	SG-8002JF-16.66700M-PCCB	EPSON	1	OSC1
OSC	SG8002JF-48.000000M-PCCB	EPSON	1	OSC2
OSC	SG8002JF-7.372800M-PCCB	EPSON	1	OSC3
OSC	SG-8002JF-22.579200M-PCCB	EPSON	1	OSC4
XTAL	MC-146 32.768kHz	EPSON	1	X1
P-Channel MOS FET	2SK2980ZZ<TL>	RENESAS	1	Q1
P-Channel MOS FET	SI3443DV-T1	VISHY	2	Q2,Q3
Transistor	2SD2150S(T100)	ROHM	1	TR1
Digital transistor	DTC1423ZE<TL>	ROHM	4	TR2-5
EMI filter	BLM18PG300SN1<D>	Murata Manufacturing	6	FL1-6
Coil	LQH55DN4R7M01L	Murata Manufacturing	1	L3
Coil	SLF6028<T>-100M1R3	TDK	1	L1
Coil	SLF10145<T>-100M2R5	TDK	1	L2

CPU Board Parts List (2)

Parts name	Model name	Maker	Quantity	Parts No.
Schottky barrier diode	CMS03	TOSHIBA	3	SD1-3
Schottky barrier diode	RB521S-30<TE61>	ROHM	1	SD4
Zener diode	U1ZB6.8<TE12L>	TOSHIBA	1	ZD1
Chip continuous resistance	MNR15E0RP-J103	ROHM	9	NR1-9
Chip resistance (1005)	MCR01MZS-J000	ROHM	12	R45 to R50, R59, R60, R62, R69, R75, and R84
Chip resistance (1005)	MCR01MZS-J101	ROHM	6	R41 to R44, R110, and R121
Chip resistance (1005)	MCR01MZS-J102	ROHM	20	R17, R19 to R23, R26, R28 to R33, R37, R52, R54 to R56, R77, and R78
Chip resistance (1005)	MCR01MZS-J103	ROHM	37	R4, R6 to R14, R16, R18, R24, R27, R34 to R36, R39, R51, R53, R57, R58, R67, R74, R79, R80, R82, R86, R87, R90, R91, R94, R95, R98, R109, R111, and R114
Chip resistance (1005)	MCR01MZS-J104	ROHM	12	R88, R89, R107, R115, R116, R118, and R124 to R128
Chip resistance (1005)	MCR01MZS-J151	ROHM	2	R96 and R97
Chip resistance (1005)	MCR01MZS-J153	ROHM	4	R100, R104, R113, and R120
Chip resistance (1005)	MCR01MZS-J164	ROHM	1	R119
Chip resistance (1005)	MCR01MZS-J202	ROHM	1	R81
Chip resistance (1005)	MCR01MZS-J222	ROHM	1	R108
Chip resistance (1005)	MCR01MZS-J224	ROHM	1	R99
Chip resistance (1005)	MCR01MZS-J330	ROHM	5	R25, R61, R92, R105, and R106
Chip resistance (1005)	MCR01MZS-J471	ROHM	6	R101, R102, R103, R112, R117 and R122
Chip resistance (1005)	MCR01MZS-J473	ROHM	1	R40
Chip resistance (1005)	MCR01MZS-J681	ROHM	1	R123
Chip resistance (1608)	MCR03MZH-J100	ROHM	4	R38, R83, R85, and R93
Chip resistance (1608)	MCR03MZH-J1R0	ROHM	3	R63, R68, and R70
Chip resistance (1608)	MCR03MZH-J221	ROHM	1	R71
Chip resistance (1608)	MCR03EZP-FX1004	ROHM	1	R73
Chip resistance (1608)	MCR03EZP-FX2003	ROHM	1	R64
Chip resistance (1608)	MCR03EZP-FX3002	ROHM	1	R65
Chip resistance (1608)	MCR03EZP-FX6203	ROHM	1	R72
Chip resistance (1608)	MCR03EZP-FX6982	ROHM	1	R2
Chip resistance (1608)	MCR03EZP-FX7872	ROHM	1	R1
Chip resistance (3216)	MCR18EZH-J101	ROHM	1	R3
Chip resistance (3216)	SR73M2B-TD 0.03ΩJ	KOA	1	R5

CPU Board Parts List (3)

Parts name	Model name	Maker	Quantity	Parts No.
Chip ceramic capacitor (1005)	GRP1552C1H100JZ01<E>	Murata Manufacturing	1	C64
Chip ceramic capacitor (1005)	GRP1552C1H101JD01<E>	Murata Manufacturing	5	C1, and C54 to C57
Chip ceramic capacitor (1005)	GRP1552C1H470JZ01<E>	Murata Manufacturing	3	C103, C107, and C114
Chip ceramic capacitor (1005)	GRP155B11H221KA01<E>	Murata Manufacturing	2	C2, C48
Chip ceramic capacitor (1005)	GRP155F11H103ZA01<E>	Murata Manufacturing	10	C8,C58,C60, C65, C67, C69, C76, C77,C83, C84,
Chip ceramic capacitor (1005)	GRP155F11C104ZA01<E>	Murata Manufacturing	51	C5, C6, C10, C14 to C21, C24, C26, C28, C32 to C34, C41, C42, C53, C59, C61, C63, C66, C70 to C72, C74, C75, C78 to C82, C88 to C91, C94 to C99, C101, C102, C104, C108, C115, and C116
Chip ceramic capacitor (1005)	GRP155F10J105ZD02<E>	Murata Manufacturing	1	C22
Chip ceramic capacitor (1608)	GRM188B11E104KA01<D>	Murata Manufacturing	6	C4, C11 to C13, C49, and C51
Chip ceramic capacitor (1608)	GRM188B11E473KA01<D>	Murata Manufacturing	1	C37
Chip ceramic capacitor (1608)	LMK107BJ105MA-T	TAIYO-YUDEN	6	C92, C93, C105, and C110 to C112
Chip ceramic capacitor (3225)	LMK325BJ106MN-T	TAIYO-YUDEN	4	C9, C27, C47, and C50
Chip ceramic capacitor (4532)	EMK432BJ226MM-T	TAIYO-YUDEN	1	C36
Tantalum electrolytic capacitor (3216)	TCFGA1A106M8R	ROHM	7	C7, C39, C68, C73, C86, C87, and C100
Tantalum electrolytic capacitor (3528)	TCFGB1A476M8R	ROHM	5	C29, C31, C44, C106, and C113
Tantalum electrolytic capacitor (2012)	TCFGP1A225M8R	ROHM	2	C23 and C109
POSCAP (D4)	4TPB470M	Sanyo Electronic Components	1	C38
POSCAP(C)	6TPB100MC	Sanyo Electric components	9	C3, C25, C30, C35, C40, C43, C45, C46 And C62
Switch	SKRELBE010	ALPS	3	SW1, SW2, and SW3
Switch	SKQDAA	ALPS	1	SW4
Switch	CHS-08B	Copal	1	SW5
Connector	RMC-EA15MY-OM15-MC1	Honda Tsushin Kogyo	1	CN1
T-Engine connector	24-5603-14-0101-861	Kyosera Elco	1	CN2
PC Card connector	31-5027-068-130-833	Kyocera Elco	1	CN3
PC Card ejector	30-5027-000-907-000	Kyocera Elco	1	For CN3
SIM Card connector	04-5036-008-110-862	Kyocera Elco	1	CN4
FPC connector	FH12-40S-0.5SH	Hirose Electric	2	CN5 and CN16
FPC connector	FH12-24S-0.5SH	Hirose Electric	1	CN6
USB connector	24-5041-0041-10-834S	Kyocera Elco	1	CN7
Connector	24-8005-002-100-867	Kyocera Elco	4	CN8, and CN11 to CN13
ϕ2.5 Jack	HSJ1602-011001	Hoshiden	2	CN9 and CN10
Power supply jack	HEC3600-010020	Hoshiden	1	CN14
FPC connector	FH12-10S-0.5SH	Hirose Electric	2	CN15 and CN17

11.1.2 LCD Board Parts List

LCD Board Parts List (1)

Parts name	Model name	Maker	Quantity	Parts No.
LCD controller	S1L50282F23K100	NEC	1	U2
Touch screen controller	ADS7843E	T.I	1	U6
DC-DC converter	LT1615ES5	LTC	3	U3-5
Remote control receiving unit	GP1UC101	SHARP	1	U1
Digital transistor	DTC143ZE<TL>	ROHM	4	TR1-4
P-ch FET	Si3443DV	VISHY	3	Q1-3
Power inductor	LQH32CN100K11L	Murata Manufacturing	3	L1-3
Push-button switch	SKRHABE010	ALPS	1	SW1
Push-button switch	SKRAAAE010	ALPS	2	SW2-3
Diode	1SS355<TE-17>	ROHM	3	D1-3
Schottky barrier diode	CRS03	TOSHIBA	6	SD1-6
Variable resistance	G4BT104	TOCOS	1	VR1
Chip resistance (1608)	MCR03EZH-J000	ROHM	2	R6 and R8
Chip resistance (1608)	MCR03EZH-J103	ROHM	9	R1-5 and R14, R16-18
Chip resistance (1608)	MCR03EZH-J124	ROHM	1	R7
Chip resistance (1608)	MCR03EZH-F1004	ROHM	2	R11 and R13
Chip resistance (1608)	MCR03EZH-F1373	ROHM	1	R10
Chip resistance (1608)	MCR03EZH-F1693	ROHM	1	R9
Chip resistance (1608)	MCR03EZH-F80R6	ROHM	1	R15
Chip resistance (1608)	MCR03EZH-F8872	ROHM	1	R12
Chip ceramic capacitor (1608)	GRM1882C1H5R0CZ01<D>	Murata Manufacturing	2	C7 and C10
Chip ceramic capacitor (1608)	GRM188B11H102KA01<D>	Murata Manufacturing	1	C22
Chip ceramic capacitor (1608)	GRM188F11E104ZA01<D>	Murata Manufacturing	10	C1-4, C9, C13, C15, C18-19, and C21
Chip ceramic capacitor (3216)	GMK316BJ105ML	TAIYO-YUDEN	1	C24
Chip ceramic capacitor (2125)	LMK212F475ZG	TAIYO-YUDEN	7	C5-6, C11,C20,C23,and C25-26
Chip ceramic capacitor (3216)	TMK316BJ105ML	TAIYO-YUDEN	4	C12,C14, C16-17
Tantalum electric capacitor (B:3528)	TCFGB1C226M8R	ROHM	1	C8
FPC connector	FH12-40S-0.5SH	HRS	1	CN1
FPC connector	FH12-24S-0.5SH	HRS	1	CN2
FPC connector	FH12-45S-0.5SH	HRS	1	CN3
FPC connector	04FLH-SM1-TB	JST	1	CN4
FPC connector	SFW4R-1STE1	FCI	1	CN5

11.1.3 Debug Board Parts List

Debug Board Parts List

Parts name	Model name	Maker	Quantity	Parts No.
LVC logic	HD74LVC245AT	RENESAS	4	U1, U2, U7, and U8
LVC logic	HD74LVC139T	RENESAS	1	U3
LVC logic	HD74LVC374AT	RENESAS	1	U5
LV1G logic	HD74LV1G32ACM	RENESAS	2	U4 and U6
8M-EPROM	MX27C8100PC-10	MXIC	1	M1
Connector	10-5603-14-0101-861	Kyocera Elco	1	CN1
Connector	DX10M-36SE	Hirose Electric	1	CN2
Short-circuit pin	FFC-2BMEP1B	Honda Tsushin Kogyo	1	J1
Jumper pin	DIC-252	Honda Tsushin Kogyo	1	(For J1)
Dip switch	CHS-08B	Copal	2	SW1 and SW2
Test pin	HK-2-S	Mac8	3	TP1-3
LED	SML-310MT	ROHM	8	LED1-8
Chip capacitor (1608)	GRM188F11E104ZA01<D>	Murata Manufacturing	5	C1-5
Chip resistance (1608)	MCR03EZH-J102	ROHM	24	R1-24

11.1.4 I/O Board Parts List

I/O Board Parts List

Parts name	Model name	Maker	Quantity	Parts No.
Chip ceramic capacitor (1608)	GRM188F11E104ZA01<D>	Murata Manufacturing	5	C1-5
Tantalum capacitor (3216)	TCFGA1A106M8R	ROHM	5	C6-10
FPC connector	FH12-40S-0.5SH	Hirose Electric	2	CN1 and CN3
FPC connector	FH12-24S-0.5SH	Hirose Electric	1	CN2
FPC connector	FH12-10S-0.5SH	Hirose Electric	1	CN4

11.2 T-Engine FPGA Logic

11.2.1 CPU Board (U11) FPGA Logic

(1)ypa5010,vhd

```
------------------------------------------------------------------------------------
--              SH7760 Solution Engine2(MS7760CP01P) FPGA
------------------------------------------------------------------------------------
--
-- module name        : CPLD(YPA5010) Top module
-- entity             : YPA5010
-- file name                        : YPA5010.vhd
--
------------------------------------------------------------------------------------
-- rev : 0    2003.01.15              Initial release
------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
------------------------------------------------------------------------------------


----------------------------------------------------------------------------
--Library
----------------------------------------------------------------------------
library IEEE;
        use IEEE.std_logic_1164.all;
        use IEEE.std_logic_unsigned.all;
----------------------------------------------------------------------------


----------------------------------------------------------------------------
--Entity
----------------------------------------------------------------------------
entity YPA5010 is
        port(
        -- from SH7760
                ShDatas         : inout std_logic_vector(31 downto 0);
                ShAddrs         : in std_logic_vector(25 downto 0);
                ShCkio          : in std_logic;
                ShCs_x          : in std_logic_vector(6 downto 0);
                ShRdWr          : in std_logic;
                ShBs_x          : in std_logic;
                ShRd_x          : in std_logic;
                ShWe_x          : in std_logic_vector(3 downto 0);

        -- from Syetem
                Rst_x           : in std_logic;

        -- from PCIC
                PcicCs_x        : out std_logic;
                PcicRst_x : out std_logic;
                PcicRdy_x: in std_logic;
                PcSirq_x        : in std_logic_vector(3 downto 0);

        -- from UART
                UartCsA_x       : out std_logic;
                UartCsB_x       : out std_logic;
                UartIntA        : in std_logic;             -- UART ChA
                UartIntB        : in std_logic;             -- UART ChB

        -- from H8/3048
                H8Irq_x         : in std_logic;

        -- from Extend Connector
                ExWait_x        : in std_logic;
                ExIrq_x         : in std_logic_vector(3 downto 0);
```

```
        -- from Debug/Extend Board
                RomSel          : in std_logic;
                Base_x          : in std_logic;

        -- from ID Switch
                IdDatas         : in std_logic_vector(5 downto 0);

        -- to pheliphe
                FlCe_x          : out std_logic;
                EpCe_x          : out std_logic;

        -- to SH7760
                ShRdy_x         : out std_logic;
                Irl_x           : out std_logic_vector(3 downto 0);

        -- to etc
                ExAddrs         : out std_logic_vector(25 downto 0);
                ExDatas         : inout std_logic_vector(31 downto 0);
                ExCkio          : out std_logic;
                ExCs2_x         : out std_logic;
                ExCs4_x         : out std_logic;
                ExCs5_x         : out std_logic;
                ExRdWr          : out std_logic;
                ExBs_x          : out std_logic;
                ExRd_x          : out std_logic;
                ExWe_x          : out std_logic_vector(3 downto 0);
                opt             : out std_logic
        );
end YPA5010;
--------------------------------------------------------------------------------



--------------------------------------------------------------------------------
--Architecture
--------------------------------------------------------------------------------
Architecture RTL of YPA5010 is

component AddrDec_r0
        port(
                ShAdr           : in std_logic_vector(25 downto 23);
                ShCs0_x         : in std_logic;
                ShCs1_x         : in std_logic;
                ShCs2_x         : in std_logic;
                ShCs4_x         : in std_logic;
                ShCs5_x         : in std_logic;
                ShCs6_x         : in std_logic;
                ShRdWr          : in std_logic;
                RomSel          :  in  std_logic;
                Base_x          : in std_logic;

                ExWait_x        : in std_logic;
                PcicRdy_x: in std_logic;

                FlCe_x          : out std_logic;
                EpCe_x          : out std_logic;
                IntRegCs        : out std_logic;
                PcicCs_x        : out std_logic;
                UartCsA_x       : out std_logic;
                UartCsB_x       : out std_logic;
                IdRegCs         : out std_logic;
```

```
                    BusEn               : out std_logic;

                    ShRdy_x             : out std_logic
          );
end component;

component IrqCnt_r0
          port(
                    PcSirq_x            : in std_logic_vector(3 downto 0);        -- MR-SHPC-01 interrupt
                    UartIntA            : in std_logic;                           -- ST16C2550 ChA interrupt
                    UartIntB            : in std_logic;                           -- ST16C2550 ChB interrupt
                    ExIrq_x             : in std_logic_vector(3 downto 0);        -- External Slot interrupt
                    H8Irq_x             : in std_logic;                           -- H8/3048 interrupt

                    IrqEna              : in std_logic_vector(3 downto 0);        -- Interrupt enable

                    Irl_x               : out std_logic_vector(3 downto 0)        -- SH7760 IRL[3:0]
          );
end component;

component IntReg_r0
          port(
                    Addrs               :  in  std_logic_vector(3 downto 1);
                    IntRegCs            : in std_logic;
                    Rd_x                          : in std_logic;
                    Wr_x                          : in std_logic;
                    WrDatas             : in std_logic_vector(3 downto 0);
                    Rst                           : in std_logic;
                    RdDatas             : out std_logic_vector(15 downto 0);
                    IrqEna              : out std_logic_vector(3 downto 0)
          );
end component;

component IdReg_r0
          port(
                    IdRegCs             : in std_logic;
                    Rd_x                          : in std_logic;
                    IdDatas             : in std_logic_vector(5 downto 0);
                    RdDatas             : out std_logic_vector(15 downto 0)
          );
end component;

component SLAddr_r0
          port(
                    ShAdr               : in std_logic_vector(25 downto 0);
                    ShCkio              : in std_logic;
                    ShCs2_x             : in std_logic;
                    ShCs4_x             : in std_logic;
                    ShCs5_x             : in std_logic;
                    ShRdWr              : in std_logic;
                    ShBs_x              : in std_logic;
                    ShRd_x              : in std_logic;
                    ShWe_x              : in std_logic_vector(3 downto 0);

                    ExAddrs             : out std_logic_vector(25 downto 0);
                    ExCkio              : out std_logic;
                    ExCs2_x             : out std_logic;
                    ExCs4_x             :  out  std_logic;
```

```
                ExCs5_x         : out std_logic;
                ExRdWr          : out std_logic;
                ExBs_x          : out std_logic;
                ExRd_x          : out std_logic;
                ExWe_x          : out std_logic_vector(3 downto 0);

                BusEn           : in std_logic;
                Base_x          : in std_logic
        );
end component;

component SLData_r0
        port(
                ShDin           : in   std_logic_vector(31 downto 0);
                ShDout          : out std_logic_vector(31 downto 0);

                ExDatas         : inout std_logic_vector(31 downto 0);

                BusEn           : in std_logic;
                RdWr                    : in std_logic
        );
end component;


------------------------------------------------------------------------------
--Signal
------------------------------------------------------------------------------
signal  IntRegCs        :std_logic;
signal  IdRegCs         :std_logic;
signal  Rst                     :std_logic;
signal  BusEn           :std_logic;

signal  IntRegDatas     :std_logic_vector(15 downto 0);
signal  IdRegDatas      :std_logic_vector(15 downto 0);
signal  ExRdDatas       :std_logic_vector(31 downto 0);
signal  IrqEna          :std_logic_vector(3  downto  0);
```

```
-------------------------------------------------------------------------------
--Function
-------------------------------------------------------------------------------
--Low hierarchy file port map

begin
          Rst                <= not Rst_x;

          ShDatas   <= (ExRdDatas or ("0000000000000000" & (IntRegDatas or IdRegDatas)))
                              when ((IntRegCs = '1' or IdRegCs ='1' or BusEn = '1' ) and ShRd_x = '0')
                              else "ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ";

          PcicRst_x <= '0' when (Rst_x = '0' or IrqEna(3) = '1')
                                         else '1';

          opt                  <= not ShCs_x(3);


U_AddrDec : AddrDec_r0 port map (
          ShAdr              => ShAddrs(25 downto 23),
          ShCs0_x            => ShCs_x(0),
          ShCs1_x            => ShCs_x(1),
          ShCs2_x            => ShCs_x(2),
          ShCs4_x            => ShCs_x(4),
          ShCs5_x            => ShCs_x(5),
          ShCs6_x            => ShCs_x(6),
          ShRdWr             => ShRdWr,

          RomSel             => RomSel,
          Base_x             => Base_x,

          ExWait_x           => ExWait_x,
          PcicRdy_x          => PcicRdy_x,

          FlCe_x            =>  FlCe_x,
          EpCe_x             => EpCe_x,
          IntRegCs           => IntRegCs,
          PcicCs_x           => PcicCs_x,
          UartCsA_x          => UartCsA_x,
          UartCsB_x          => UartCsB_x,
          IdRegCs            => IdRegCs,

          BusEn              => BusEn,

          ShRdy_x            => ShRdy_x
);
U_IrqCnt : IrqCnt_r0 port map (
          PcSirq_x           => PcSirq_x,
          UartIntA           => UartIntA,
          UartIntB           => UartIntB,
          ExIrq_x            => ExIrq_x,
          H8Irq_x            => H8Irq_x,

          IrqEna             => IrqEna,

          Irl_x              => Irl_x
);
```

```
U_IntReg : IntReg_r0 port map (
        Addrs           => ShAddrs(3 downto 1),
        IntRegCs        => IntRegCs,
        Rd_x            => ShRd_x,
        Wr_x            => ShWe_x(0),
        WrDatas         => ShDatas(3 downto 0),
        Rst             => Rst,
        RdDatas         => IntRegDatas,
        IrqEna          => IrqEna
);

U_IdReg : IdReg_r0 port map (
        IdRegCs         => IdRegCs,
        Rd_x                    => ShRd_x,
        IdDatas         => IdDatas,
        RdDatas         => IdRegDatas
);

U_SLAddr : SLAddr_r0 port map (
        ShAdr           => ShAddrs,
        ShCkio          => ShCkio,
        ShCs2_x         => ShCs_x(2),
        ShCs4_x         => ShCs_x(4),
        ShCs5_x         => ShCs_x(5),
        ShRdWr          => ShRdWr,
        ShBs_x          => ShBs_x,
        ShRd_x          => ShRd_x,
        ShWe_x          => ShWe_x,

        ExAddrs         => ExAddrs,
        ExCkio          => ExCkio,
        ExCs2_x         => ExCs2_x,
        ExCs4_x         => ExCs4_x,
        ExCs5_x         => ExCs5_x,
        ExRdWr          => ExRdWr,
        ExBs_x          => ExBs_x,
        ExRd_x          => ExRd_x,
        ExWe_x          => ExWe_x,

        BusEn           => BusEn,
        Base_x          => Base_x
);

U_SLData : SLData_r0 port map (
        ShDin           => ShDatas,
        ShDout          => ExRdDatas,
        ExDatas         => ExDatas,
        BusEn           => BusEn,
        RdWr            => ShRdWr
);

end RTL;
```

(2)AddrDec_r0.vhd

```
-------------------------------------------------------------------------------------
--		SH7760 Solution Engine2(MS7760CP01P) FPGA
-------------------------------------------------------------------------------------
--
-- module name	: Address Decoder for MS7760CP01P/0
-- entity		: AddrDec_r0
-- file name			: AddrDec_r0.vhd
--
-------------------------------------------------------------------------------------
-- rev : 0	2003.01.15		Initial release
-------------------------------------------------------------------------------------
- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
-------------------------------------------------------------------------------------
library IEEE;
		use IEEE.std_logic_1164.all;
		use IEEE.std_logic_unsigned.all;


entity AddrDec_r0 is
		port(
				ShAdr			: in std_logic_vector(25 downto 23);
				ShCs0_x			: in std_logic;
				ShCs1_x			: in std_logic;
				ShCs2_x			: in std_logic;
				ShCs4_x			: in std_logic;
				ShCs5_x			: in std_logic;
				ShCs6_x			: in std_logic;
				ShRdWr			: in std_logic;

				RomSel			: in std_logic;
				Base_x			: in std_logic;

				ExWait_x		: in std_logic;
				PcicRdy_x		:  in  std_logic;
				FlCe_x			: out std_logic;
				EpCe_x			: out std_logic;
				IntRegCs		: out std_logic;
				PcicCs_x		: out std_logic;
				UartCsA_x		: out std_logic;
				UartCsB_x		: out std_logic;
				IdRegCs			: out std_logic;

				BusEn			: out std_logic;

				ShRdy_x			: out std_logic
		);
end AddrDec_r0;

Architecture RTL of AddrDec_r0 is
begin
-- decode
		FlCe_x	<=  '0'  when  ((ShCs0_x = '0' and Base_x = '1' and ShAdr(25) = '0' and ShAdr(24) = '0')
```

```
                              or  (ShCs0_x = '0' and Base_x = '0' and RomSel = '1' and ShAdr(25) = '0' and ShAdr(24) = '0')
                              or  (ShCs0_x = '0' and Base_x = '0' and RomSel = '0' and ShAdr(25) = '0' and ShAdr(24) = '1'))
                                              else '1';

        EpCe_x    <= '0' when ((ShCs0_x = '0' and Base_x = '0' and RomSel = '1' and ShAdr(25) = '0' and ShAdr(24) = '1')
                              or  (ShCs0_x = '0' and Base_x = '0' and RomSel = '0' and ShAdr(25) = '0' and ShAdr(24) = '0'))
                                              else '1';

        IntRegCs  <= '1' when  (ShCs1_x = '0')
                                              else '0';

        PcicCs_x  <= '0' when  (ShCs6_x = '0' and ShAdr(25) = '0')
                                              else '1';

        UartCsA_x <= '0' when  (ShCs6_x = '0' and ShAdr = B"100")
                                              else '1';

        UartCsB_x <= '0' when  (ShCs6_x = '0' and ShAdr = B"101")
                                              else '1';

        IdRegCs   <= '1' when  (ShCs6_x = '0' and ShAdr(25) = '1' and ShAdr(24) = '1')
                                              else '0';

        BusEn      <= '1' when ((ShCs0_x = '0' and Base_x = '0' and RomSel = '1' and ShAdr(25) = '0' and ShAdr(24) = '1')
                              or   (ShCs0_x = '0' and Base_x = '0' and RomSel = '0' and ShAdr(25) = '0' and ShAdr(24) = '0')
                              or  (ShCs2_x = '0' and Base_x = '0')
                              or  (ShCs4_x = '0' and Base_x = '0')
                              or  (ShCs5_x = '0' and Base_x = '0'))
                                              else '0';
        ShRdy_x   <= '1' When ((ExWait_x  = '0' and ShCs2_x = '0' and Base_x = '0')
                              or  (ExWait_x  = '0' and ShCs4_x = '0' and Base_x = '0')
                              or  (ExWait_x  = '0' and ShCs5_x = '0' and Base_x = '0')
                              or  (PcicRdy_x = '1' and ShCs6_x = '0' and ShAdr(25) = '0'))
                                              else '0';

end RTL;
```

(3)IrqCnt_r0.vhd

```
----------------------------------------------------------------------------------------
--              SH7760 Solution Engine2(MS7760CP01P) FPGA
----------------------------------------------------------------------------------------
--
-- module name       : Interrupt Controler for MS7760CP01P/0
-- entity            : IrqCnt_r0
-- file name                    : IrqCnt_r0.vhd
--
----------------------------------------------------------------------------------------
-- rev : 0    2003.01.28             Initial release
----------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
----------------------------------------------------------------------------------------
library IEEE;
                use IEEE.std_logic_1164.all;
                use IEEE.std_logic_unsigned.all;


entity IrqCnt_r0 is
                port(
-- Interrupt input
                                PcSirq_x        : in std_logic_vector(3 downto 0);      -- MR-SHPC-01 interrupt
                                UartIntA        : in std_logic;                         -- ST16C2550 ChA interrupt
                                UartIntB        : in std_logic;                         -- ST16C2550 ChB interrupt
                                ExIrq_x         : in std_logic_vector(3 downto 0);      -- External Slot interrupt
                                H8Irq_x         : in std_logic;                         -- H8/3048 interrupt
-- Interrupt Enable input
                                IrqEna          : in std_logic_vector(3 downto 0);      -- Interrupt enable
-- Interrupt output
                                Irl_x           : out std_logic_vector(3 downto 0)
                );
end IrqCnt_r0;

Architecture RTL of IrqCnt_r0 is
```

```
signal   Irl        : std_logic_vector(3 downto 0);

begin
-- External slot interrupt
         process(PcSirq_x, UartIntA, UartIntB, ExIrq_x, H8Irq_x, IrqEna)
         begin
                  if     ExIrq_x(3)   = '0'                          then      Irl <= X"F";      -- Level 15
                  elsif  PcSirq_x(3)  = '0'                          then      Irl <= X"E";      -- Level 14
                  elsif (H8Irq_x      = '0' and IrqEna(0) = '1')     then      Irl <= X"D";      -- Level 13
                  elsif  UartIntB     = '1'                          then      Irl <= X"C";      -- Level 12
                  elsif  ExIrq_x(2)   = '0'                          then      Irl <= X"B";      -- Level 11
                  elsif  PcSirq_x(2)  = '0'                          then      Irl <= X"A";      -- Level 10
                  elsif  UartIntA     = '1'                          then      Irl <= X"9";      -- Level  9
                  elsif  ExIrq_x(1)   = '0'                          then      Irl <= X"8";      -- Level  8
                  elsif  PcSirq_x(1)  = '0'                          then      Irl <= X"7";      -- Level  7
                  elsif  ExIrq_x(0)   = '0'                          then      Irl <= X"6";      -- Level  6
                  elsif  PcSirq_x(0)  = '0'                          then      Irl <= X"5";      -- Level  5
                  else                                                         Irl <= X"0";      -- Level  0
                  end if;
         end process;

         Irl_x        <= not Irl;

end RTL;
```

(4)IntReg_r0.vhd

```
-----------------------------------------------------------------------------------------
--              SH7760 Solution Engine2(MS7760CP01P) FPGA
-----------------------------------------------------------------------------------------
--
-- module name      : Internal register
-- entity           : IntReg_r0
-- file name                   : IntReg_r0.vhd
--
-----------------------------------------------------------------------------------------
-- rev : 0    2003.01.15              Initial release
-----------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
-----------------------------------------------------------------------------------------
library IEEE;
        use IEEE.std_logic_1164.all;
        use IEEE.std_logic_unsigned.all;

entity IntReg_r0 is
        port(
                Addrs           : in std_logic_vector(3 downto 1);
                IntRegCs        : in std_logic;
                Rd_x            : in std_logic;
                Wr_x            : in std_logic;
                WrDatas         : in std_logic_vector(3 downto 0);
                Rst             : in std_logic;
                RdDatas         : out std_logic_vector(15 downto 0);
                IrqEna          : out std_logic_vector(3 downto 0)
        );
end IntReg_r0;

Architecture RTL of IntReg_r0 is

constant        RegRD0          : std_logic_vector(15 downto 0) := X"0000";     -- 0x0000(Initial value)
constant        FpgaId0         : std_logic_vector(15 downto 0) := X"5950";     -- 0x5950(Y P)
constant        FpgaId1         : std_logic_vector(15 downto 0) := X"4135";     -- 0x4135(A 5)
constant        FpgaId2         : std_logic_vector(15 downto 0) := X"3031";     -- 0x3031(0 1)
constant        FpgaId3         : std_logic_vector(15 downto 0) := X"3000";     -- 0x3200(0 Null)

signal          IrqEnaReg       :std_logic_vector(3 downto 0);
signal          RegWr           :std_logic;

begin

RegWr <= '1' when (Addrs = "000" and IntRegCs = '1' and Wr_x = '0')
                                else  '0';

IrqEna <= IrqEnaReg;

        process(Addrs, IntRegCs, Rd_x, IrqEnaReg)
        begin
                if (IntRegCs = '1' and Rd_x = '0') then
                        case Addrs is
```

```
                    when "000"  => RdDatas <= (X"000" & IrqEnaReg); -- Interrupt control register
                    when "100"  => RdDatas <= FpgaId0;                  -- 0x5950(Y P)
                    when "101"  => RdDatas <= FpgaId1;                  -- 0x4135(A 5)
                    when "110"  => RdDatas <= FpgaId2;                  -- 0x3031(0 1)
                    when "111"  => RdDatas <= FpgaId3;                  -- 0x3000(0 Null)
                    when others => RdDatas <= RegRD0;
                    end case;
            else RdDatas <= RegRD0;
            end if;
    end process;


-- Interrupt control register
    process(RegWr, WrDatas, Rst)
    begin
            if(Rst ='1') then
                    IrqEnaReg <= "0000";
            elsif (RegWr'event and RegWr = '0') then
                    IrqEnaReg <= WrDatas;
            end if;
    end process;

end RTL;
```

(5)IdReg_r0.vhd

```
-----------------------------------------------------------------------------------------
--		SH7760 Solution Engine2(MS7760CP01P) FPGA
-----------------------------------------------------------------------------------------
--
-- module name		: ID register
-- entity			: IdReg_r0
-- file name		: IdReg_r0.vhd
--
-----------------------------------------------------------------------------------------
-- rev : 0	2003.01.15		Initial release
-----------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
-----------------------------------------------------------------------------------------
library IEEE;
		use IEEE.std_logic_1164.all;
		use IEEE.std_logic_unsigned.all;


entity IdReg_r0 is
		port(
			IdRegCs			:	in std_logic;
			Rd_x					:	in std_logic;
			IdDatas			:	in std_logic_vector(5 downto 0);
			RdDatas			: out std_logic_vector(15 downto 0)
		);
end IdReg_r0;


Architecture RTL of IdReg_r0 is

begin

		process(IdRegCs, Rd_x, IdDatas)
		begin
			if	(IdRegCs = '1' and Rd_x = '0') then RdDatas <= (X"00" & B"00" & IdDatas);	--	MODE	setting
DIP-SW Read
(MDSW(5:0))
			else						RdDatas <= X"0000";
			end if;
		end process;

end RTL;
```

(6)SLAddr_r0.vhd

```
---------------------------------------------------------------------------------------
--              SH7760 Solution Engine2(MS7760CP01P) FPGA
---------------------------------------------------------------------------------------
--
-- module name      : SH Local Address/Control Bus Interface in Extend Connector
-- entity           : SLAddr_r0
-- file name        : SLAddr_r0.vhd
--
---------------------------------------------------------------------------------------
-- rev : 0    2003.01.27              Initial release
---------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
---------------------------------------------------------------------------------------
library IEEE;
        use IEEE.std_logic_1164.all;
        use IEEE.std_logic_unsigned.all;


entity SLAddr_r0 is
        port(
        -- from SH side
                ShAdr           : in std_logic_vector(25 downto 0);
                ShCkio          : in std_logic;
                ShCs2_x         : in std_logic;
                ShCs4_x         : in std_logic;
                ShCs5_x         : in std_logic;
                ShRdWr          : in std_logic;
                ShBs_x          : in std_logic;
                ShRd_x          : in std_logic;
                ShWe_x          : in std_logic_vector(3 downto 0);

        -- from Extend Connector
                ExAddrs         : out std_logic_vector(25 downto 0);
                ExCkio          : out std_logic;
                ExCs2_x         : out std_logic;
                ExCs4_x         : out std_logic;
                ExCs5_x         : out std_logic;
                ExRdWr          : out std_logic;
                ExBs_x          : out std_logic;
                ExRd_x          : out std_logic;
                ExWe_x          : out std_logic_vector(3 downto 0);

        -- from Controler
                BusEn           : in std_logic;
                Base_x          : in std_logic
        );
end SLAddr_r0;

Architecture RTL of SLAddr_r0 is
begin
        ExAddrs   <= ShAdr        when (BusEn = '1')
                                  else "00000000000000000000000000";

        ExCkio    <= ShCkio       when (Base_x = '0')
                                  else '1';

        ExCs2_x   <= ShCs2_x      when (Base_x = '0')
                                  else '1';
```

```
        ExCs4_x    <=  ShCs4_x        when (Base_x = '0')
                                      else '1';

        ExCs5_x    <=  ShCs5_x        when (Base_x = '0')
                                      else '1';

        ExRdWr     <=  ShRdWr         when (Base_x = '0')
                                      else '1';

        ExBs_x     <=  ShBs_x         when (Base_x= '0')
                                      else '1';

        ExRd_x     <=  ShRd_x         when (Base_x= '0')
                                      else '1';

        ExWe_x     <=  ShWe_x         when (Base_x = '0')
                                      else "1111";

end RTL;
```

(7)SLData_r0.vhd

```
--------------------------------------------------------------------------------------
--              SH7760 Solution Engine2(MS7760CP01P) FPGA
--------------------------------------------------------------------------------------
--
-- module name        : SH Local Data Bus Interface in Extend Connector
-- entity             : SLData_r0
-- file name          : SLData_r0.vhd
--
--------------------------------------------------------------------------------------
-- rev : 0    2003.01.27              Initial release
--------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
--------------------------------------------------------------------------------------
library IEEE;
        use IEEE.std_logic_1164.all;
        use IEEE.std_logic_unsigned.all;


entity SLData_r0 is
        port(
        -- from SH side
                ShDin               : in   std_logic_vector(31 downto 0);
                ShDout              : out std_logic_vector(31 downto 0);

        -- from Extend Connector
                ExDatas             : inout std_logic_vector(31 downto 0);

        -- from Controler
                BusEn               : in std_logic;
                RdWr                : in std_logic
        );
end SLData_r0;


Architecture RTL of SLData_r0 is
begin
        ExDatas <= ShDin    when (BusEn = '1' and RdWr = '0')
                            else "ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ";

        ShDout   <=  ExDatas            when (BusEn = '1' and RdWr = '1')
                                        else "00000000000000000000000000000000";

end RTL;
```

(1)ypa5020,vhd

```
--------------------------------------------------------------------------------
--		SH7760 Solution Engine2(MS7760CP01P) FPGA
--------------------------------------------------------------------------------
--
-- module name		: CPLD(YPA5020) Top module
-- entity			: YPA5020
-- file name			: YPA5020.vhd
--
--------------------------------------------------------------------------------
-- rev : 0	2003.01.28		Initial release
--------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
--------------------------------------------------------------------------------


-------------------------------------------------------------------------
--Library
-------------------------------------------------------------------------
library IEEE;
		use IEEE.std_logic_1164.all;
		use IEEE.std_logic_unsigned.all;
-------------------------------------------------------------------------



-------------------------------------------------------------------------
--Entity
-------------------------------------------------------------------------
entity YPA5020 is
		port(
		-- from SH7760
				ShExtal			: in std_logic;

		-- form ROM-ICE I/F
				ExRstIn_x : in std_logic;
				ExNmiIn			: in std_logic;
				H8Rst_x			: in std_logic;

		-- from H8/3048
				ShRst_x			: in std_logic;
				ShNmiIn			: in std_logic;

		-- to SH7760
				ShNmiOut: out std_logic;

		-- to etc
				Rst					: out std_logic;
				Rst_x			: out std_logic_vector(2 downto 0);
				MdSel			: out std_logic
		);
end YPA5020;
-------------------------------------------------------------------------
```

```
------------------------------------------------------------------------------
--Architecture
------------------------------------------------------------------------------
Architecture RTL of YPA5020 is

component RstCnt_r0
        port(
                ShExtal         : in std_logic;
                ExRstIn_x : in std_logic;
                ShRst_x         : in std_logic;
                H8Rst_x         : in std_logic;

                RstOut          : out std_logic;
                MdSel           : out std_logic
        );
end component;

------------------------------------------------------------------------------
--Signal
------------------------------------------------------------------------------
signal  RstOut          :std_logic;


------------------------------------------------------------------------------
--Function
------------------------------------------------------------------------------
--Low hierarchy port map

begin

--Reset
        Rst_x   <= "000" when (RstOut = '1')
                        else "111";
        Rst     <= RstOut;

-- NMI
        ShNmiOut <= '0' when (ShNmiIn = '0'
                        or   ExNmiIn  =  '0')
                        else '1';

U_RstCnt : RstCnt_r0 port map (
        ShExtal         => ShExtal,
        ExRstIn_x       => ExRstIn_x,
        ShRst_x         => ShRst_x,
        H8Rst_x         => H8Rst_x,

        RstOut          => RstOut,
        MdSel           => MdSel
);

end RTL;
```

(2) RstCnt_r0.vhd

```
-------------------------------------------------------------------------------------
--            SH7760 Solution Engine2(MS7760CP01P) FPGA
-------------------------------------------------------------------------------------
--
-- module name       : Reset control for MS7760CP01P/0
-- entity            : RstCnt_r0
-- file name         : RstCnt_r0.vhd
--
-------------------------------------------------------------------------------------
-- rev : 0    2003.01.15             Initial release
-------------------------------------------------------------------------------------
-- (c) copyright Hitachi ULSI Systems Co.,Ltd. 2003
-------------------------------------------------------------------------------------
library IEEE;
            use IEEE.std_logic_1164.all;
            use IEEE.std_logic_unsigned.all;

entity RstCnt_r0 is
            port(
                        ShExtal               : in std_logic;
                        ExRstIn_x             : in std_logic;
                        ShRst_x               : in std_logic;
                        H8Rst_x               : in std_logic;

                        RstOut                : out std_logic;
                        MdSel                 : out std_logic
            );
end RstCnt_r0;


Architecture RTL of RstCnt_r0 is

signal      MdSel_r    :std_logic;
begin

--Reset control
            RstOut <= '1' When (ExRstIn_x = '0'
                                          or   ShRst_x    = '0'
                                          or   H8Rst_x    = '0')
                                          else '0';

            process(ShExtal, ExRstIn_x, ShRst_x, H8Rst_x)
            begin
                        if(ExRstIn_x = '0' or ShRst_x ='0' or H8Rst_x ='0') then
                                    MdSel_r <= '0';
                        elsif (ShExtal'event and ShExtal = '1') then
                                    MdSel_r <= '1';
                        end if;
            end process;

            process(ShExtal)
            begin
                        if (ShExtal'event and ShExtal = '1') then
                                    MdSel <= MdSel_r;
                        end if;
            end process;

end RTL;
```

11.3 T-Engine Board Circuit Diagrams

11.3.1 CPU Board Circuit Diagrams (MS7760CP01/1)

11.3.2 LCD Board Circuit Diagrams (MS7760LCD01/4)

11.3.3 Debug Board Circuit Diagrams (MS7760DBG01/3)

11.3.4 I/O Board Circuit Diagrams

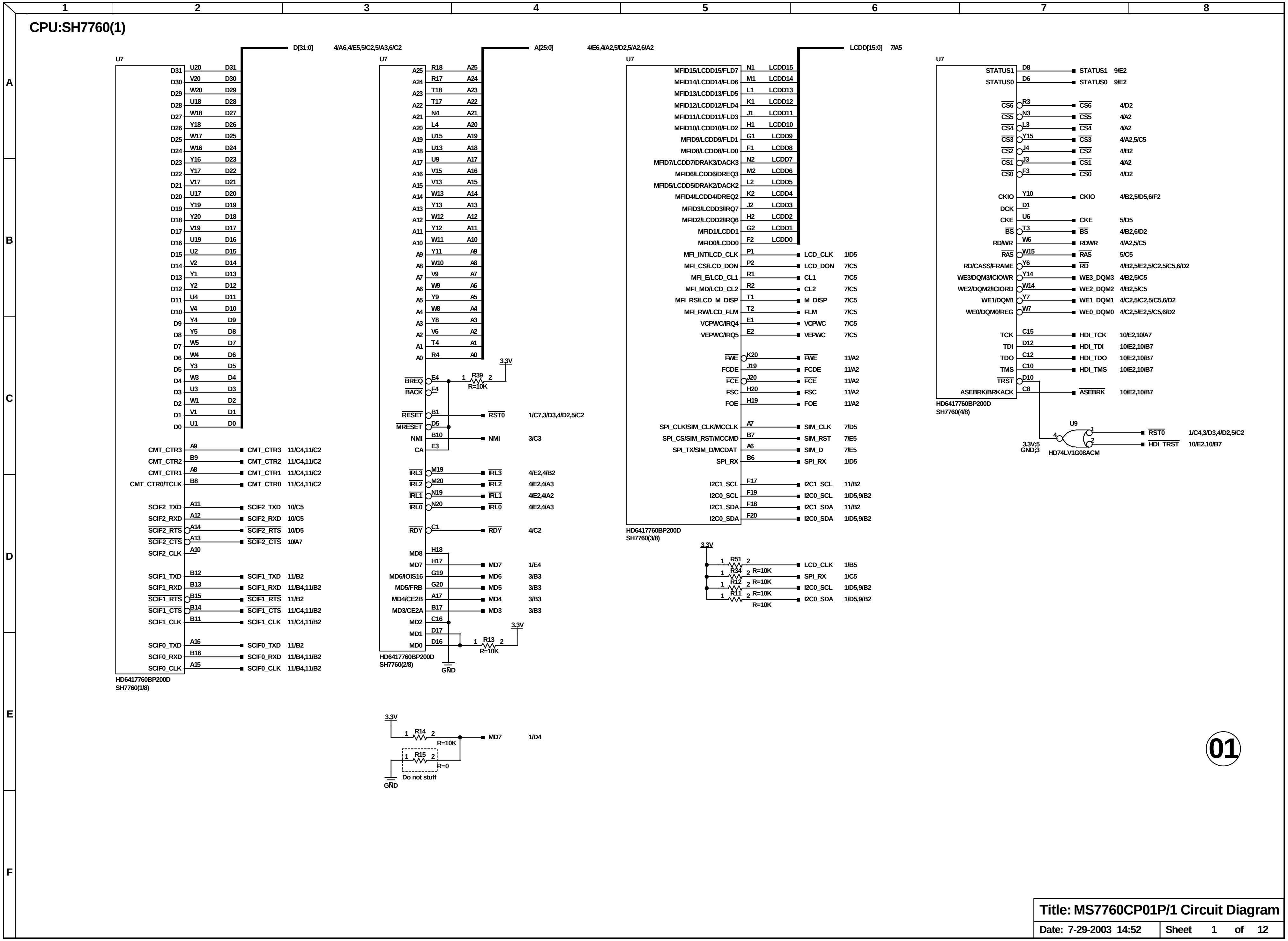
11.4 T-Engine Board Dimensions

11.4.1 CPU Board (MS7760CP01/3) Dimensions

11.4.2 LCD Board (MS7760LCD01/4) Dimensions

11.4.3 Debug Board (MS7760DBG01/3) Dimensions

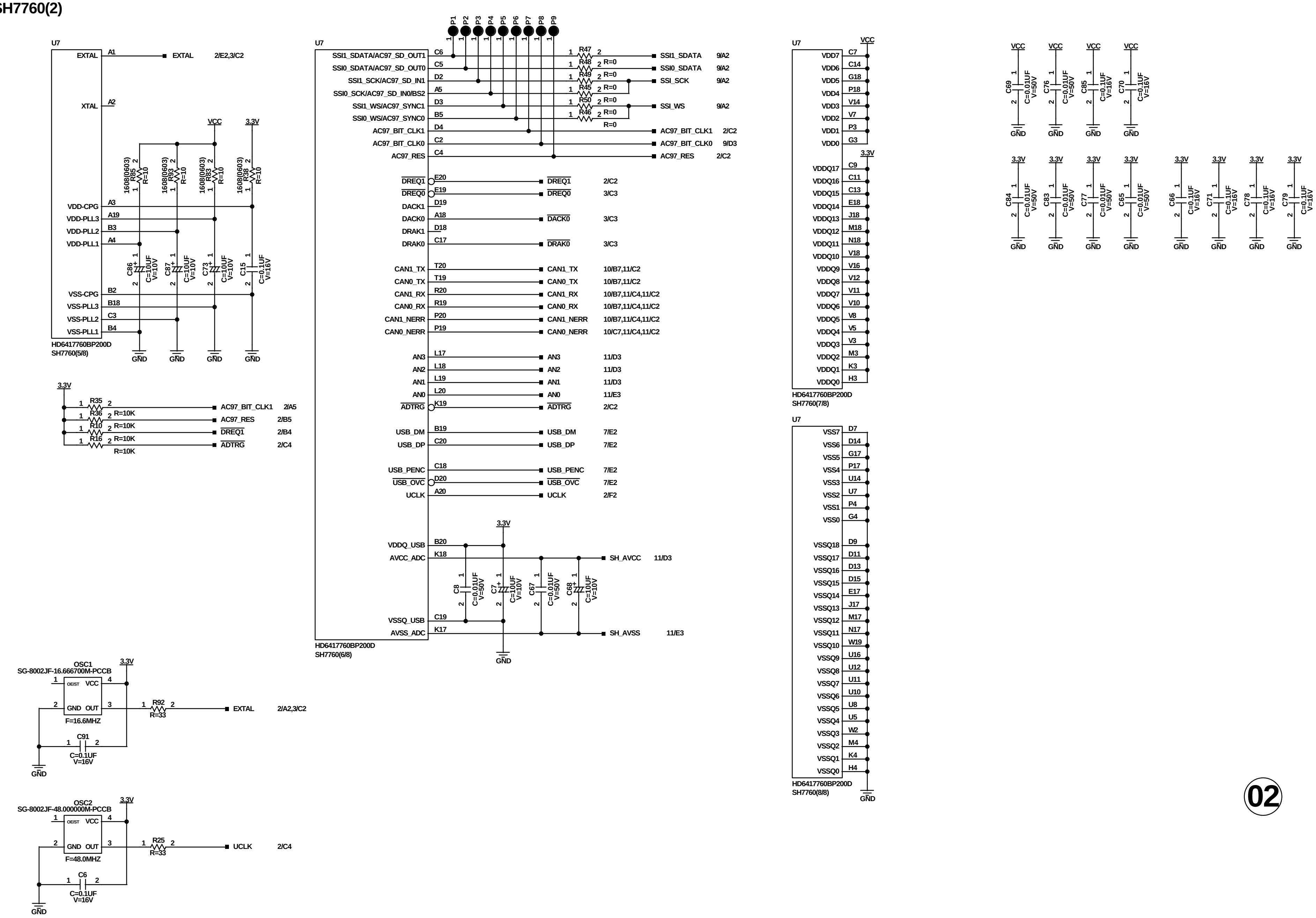
CPU:SH7760(1)



Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 1 of 12

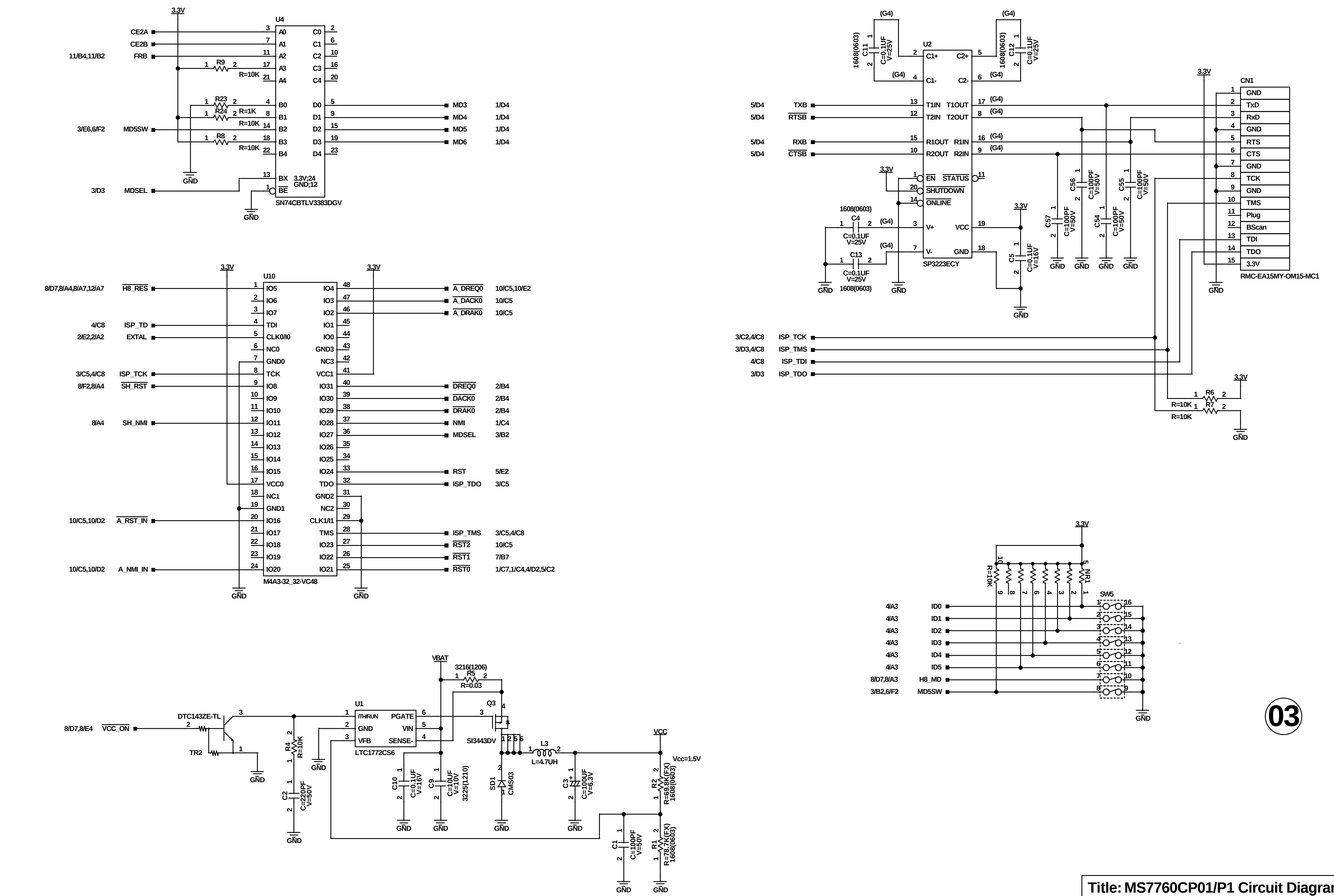
CPU:SH7760(2)



Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 2 of 12

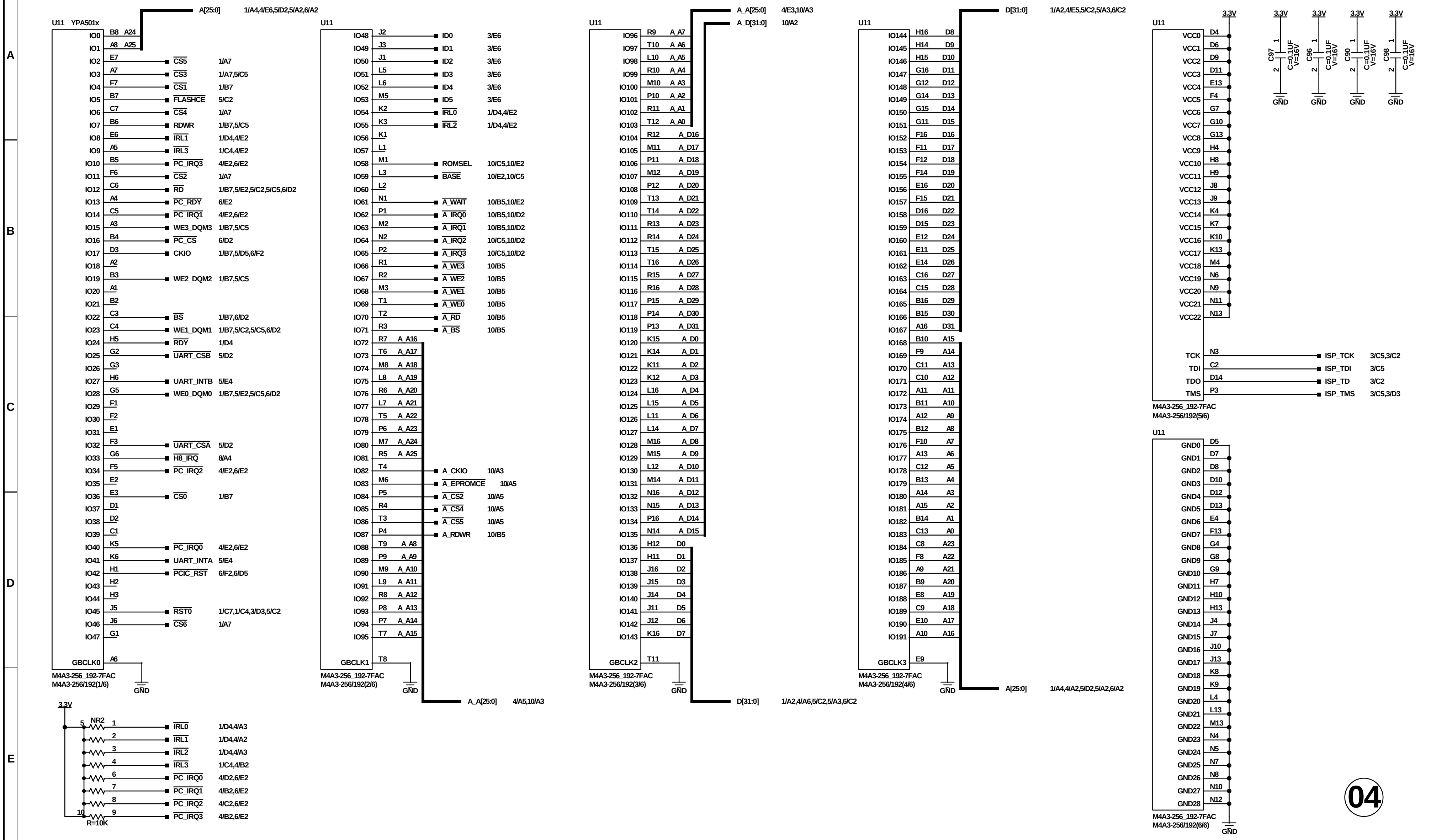
SH7760 MODE CONTROL & SIRIAL I/F



Title: MS7760CP01/P1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 3 of 12

CPLD

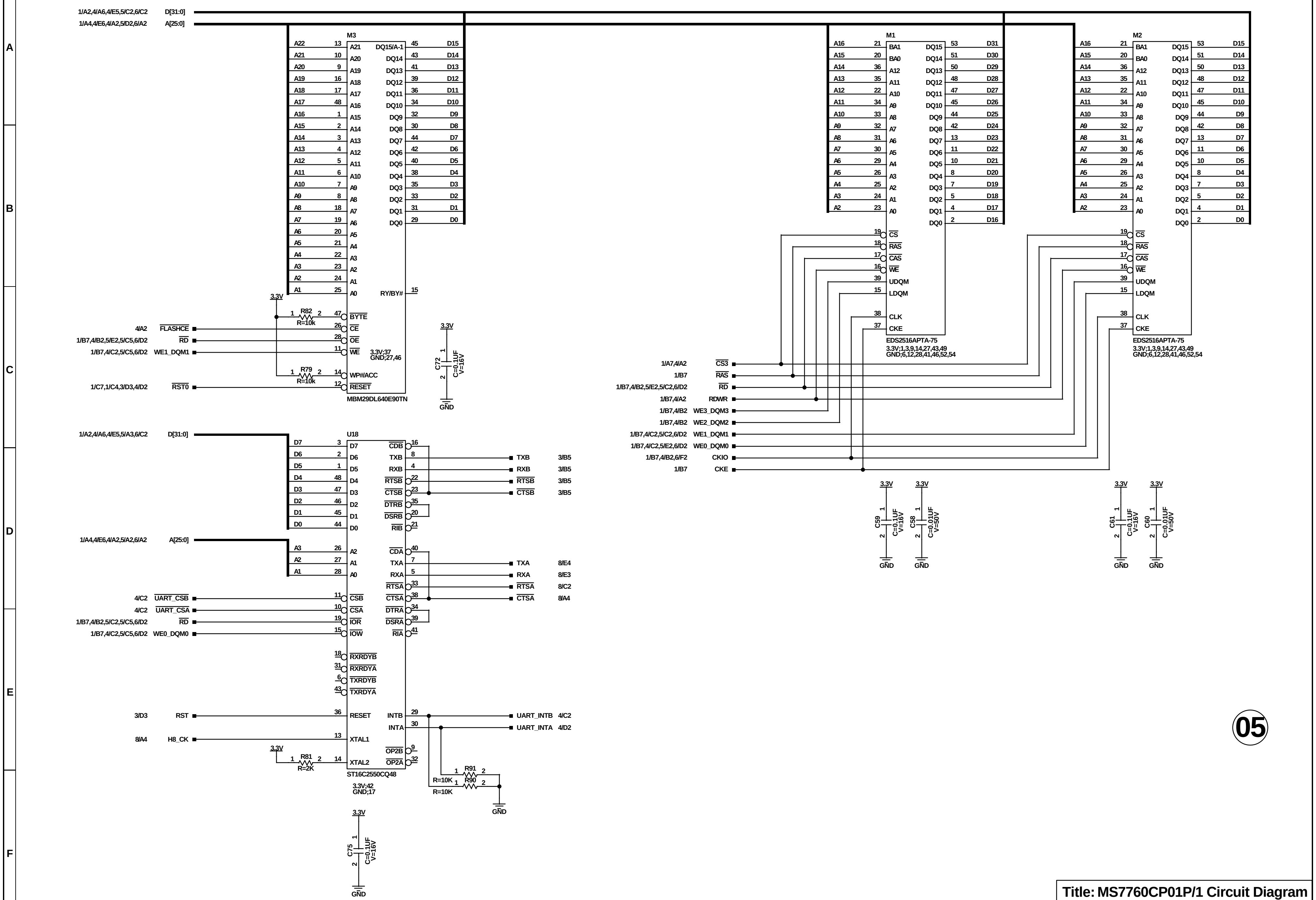


Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 4 of 12

04

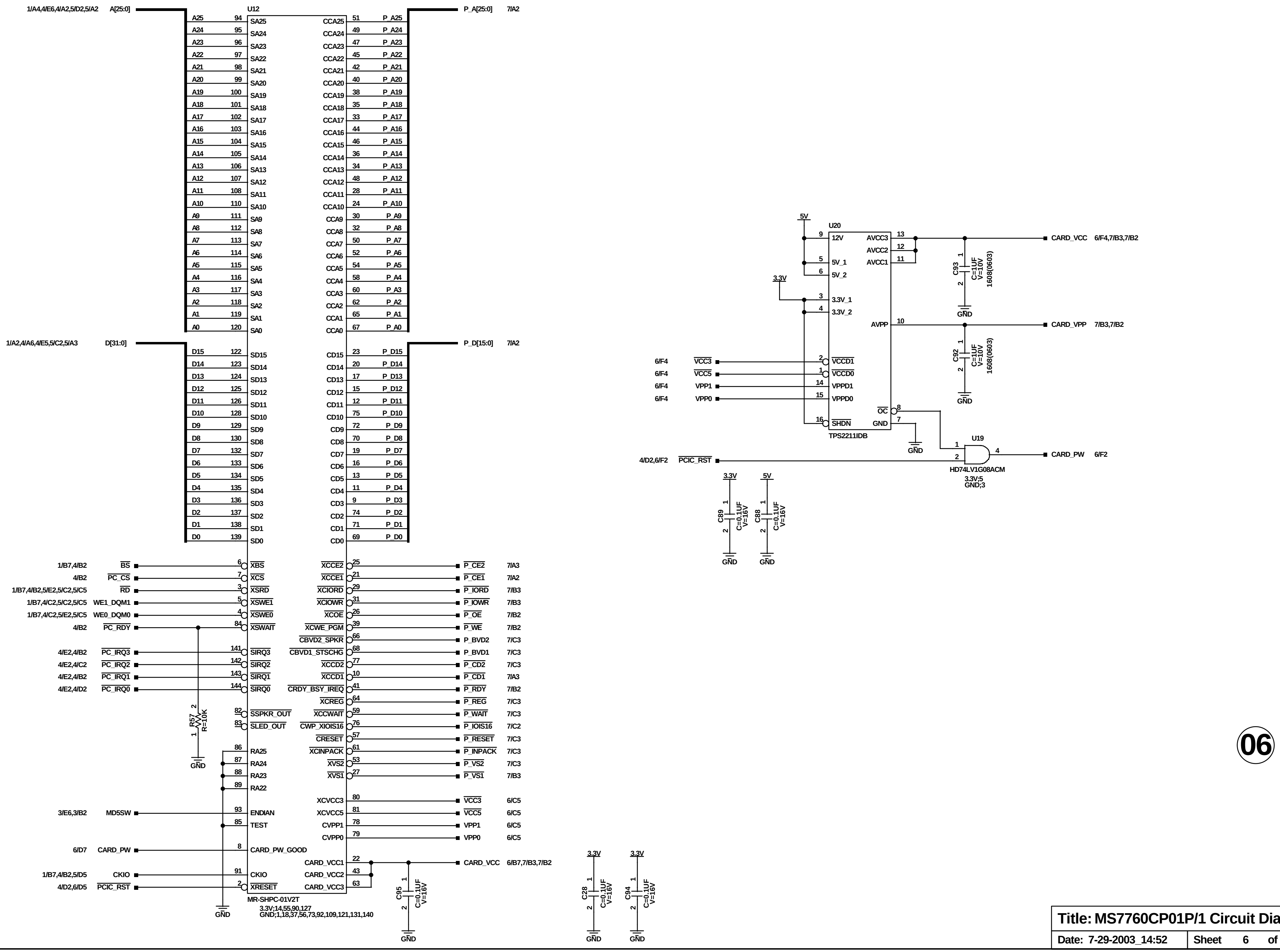
FLASH MEMORY&SDRAM



Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 5 of 12

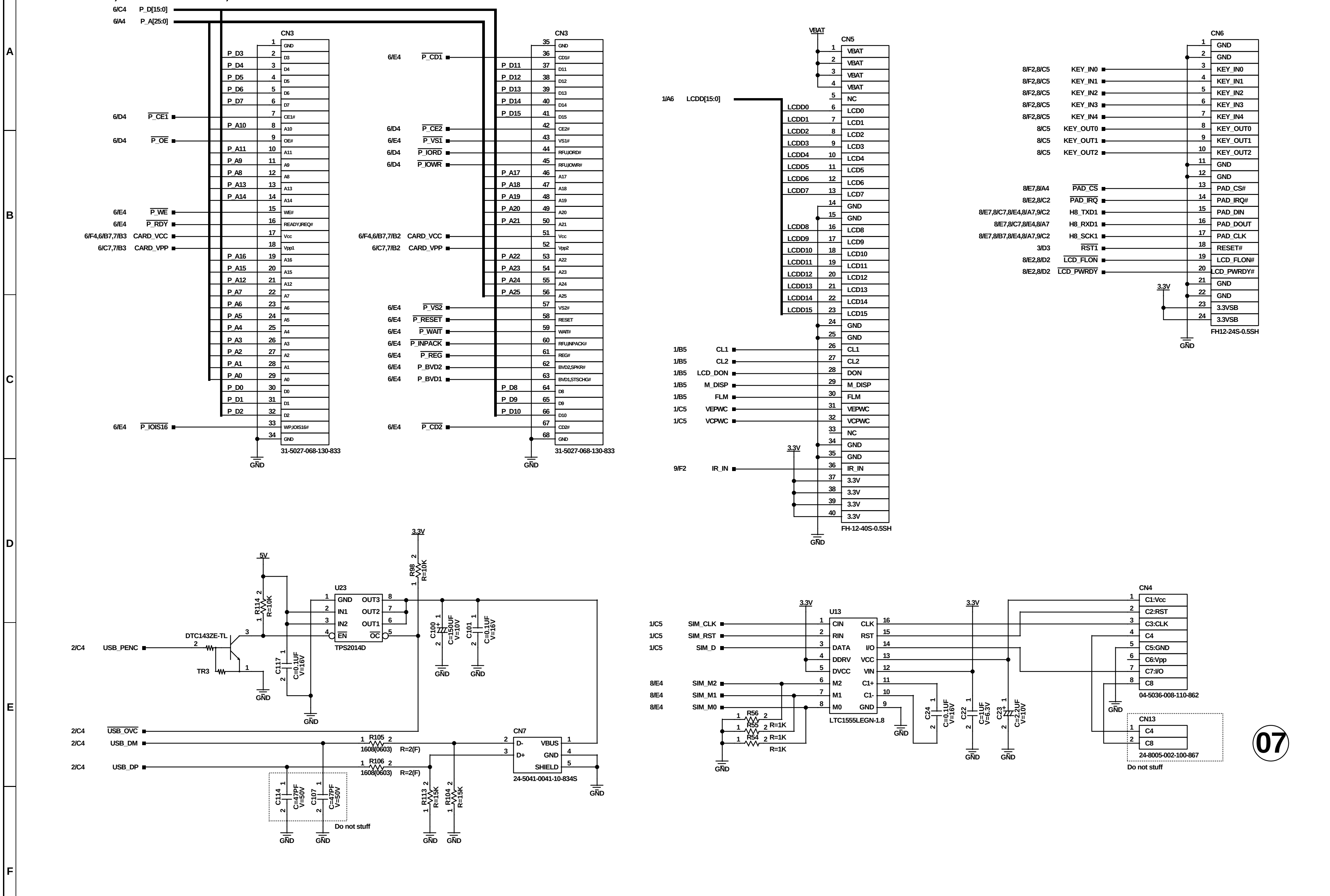
PC CARD I/F CONTROLER



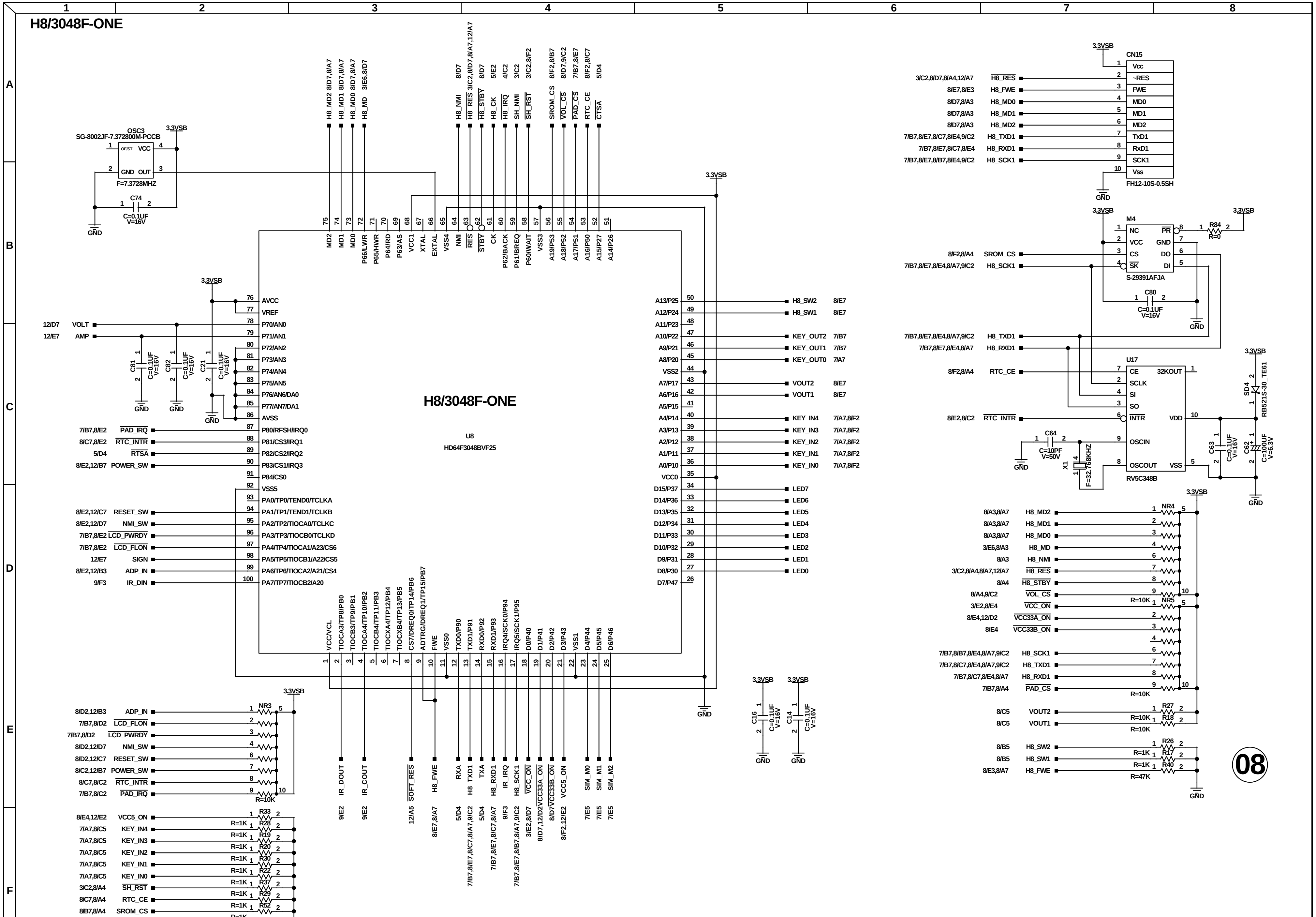
Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 6 of 12

PC CARD I/F,USB I/F&LCD I/F,SIM CARD I/F

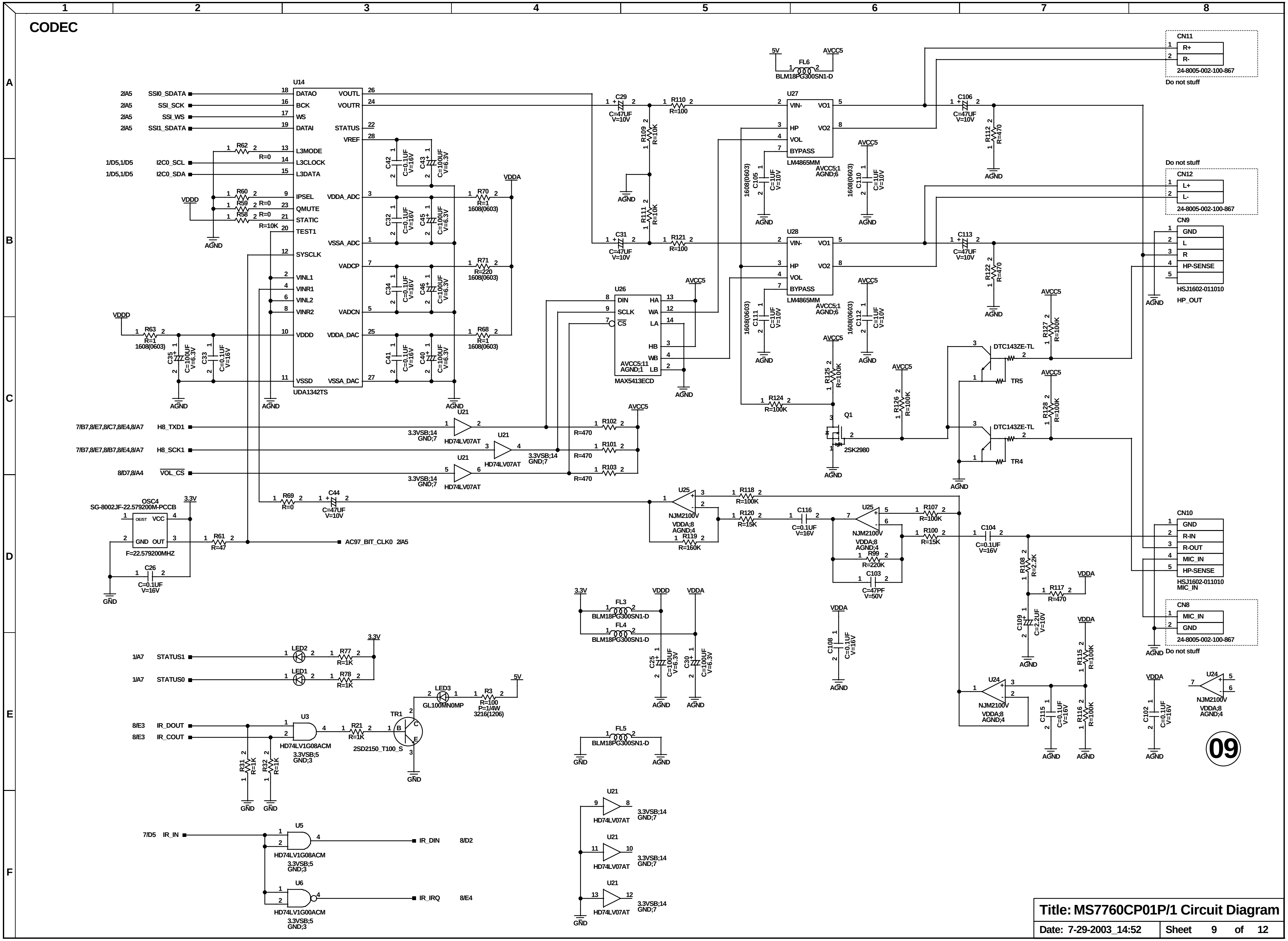


Title: MS7760CP01P/1 Circuit Diagram	
Date: 7-29-2003_14:52	Sheet 7 of 12

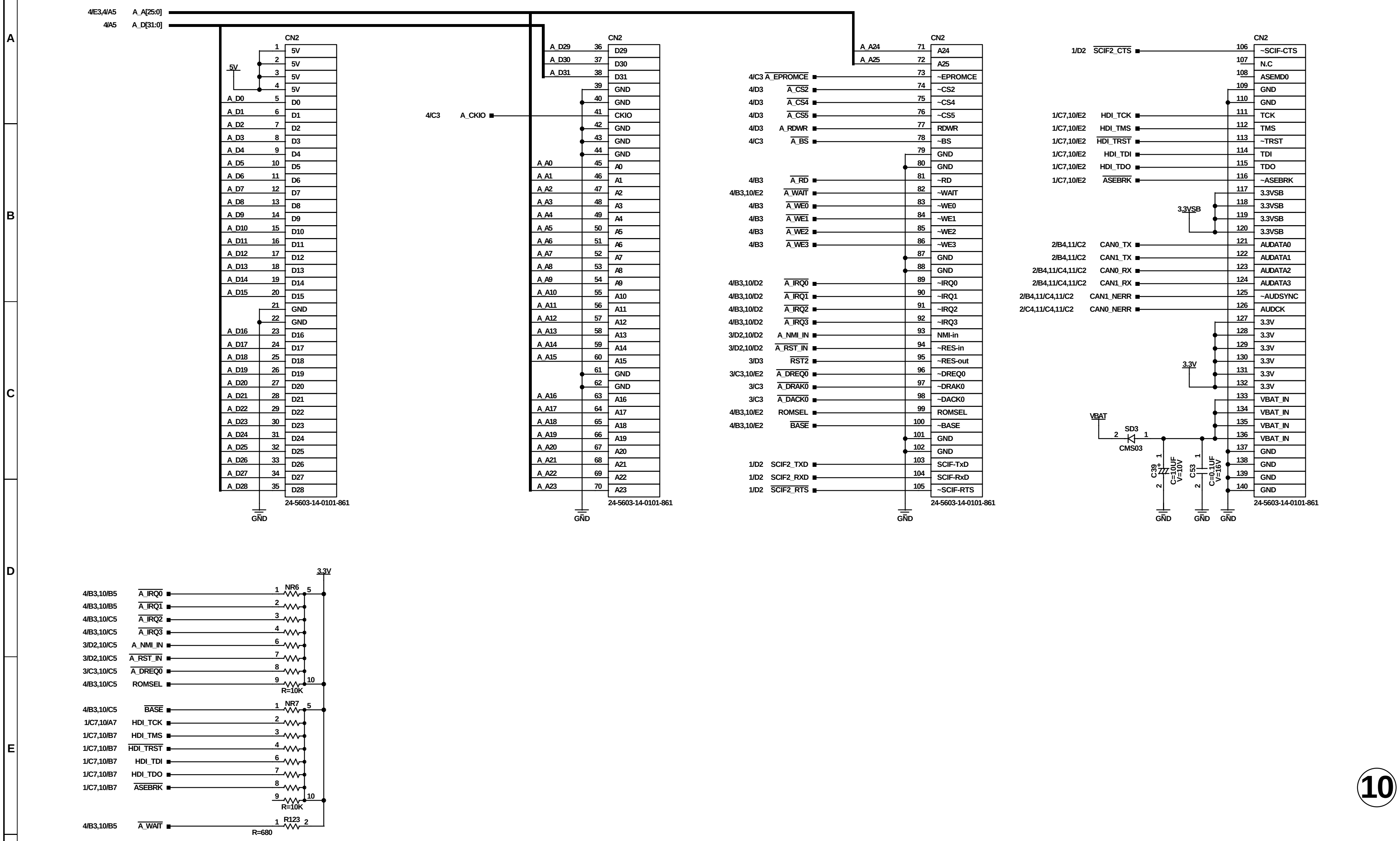


Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52 | Sheet 8 of 12


CODEC
U14
UDA1342TS
SSI0_SDATA
SSI_SCK
SSI_WS
SSI1_SDATA
I2C0_SCL
I2C0_SDA
DATAO
BCK
WS
DATAI
L3MODE
L3CLOCK
L3DATA
IPSEL
QMUTE
STATIC
TEST1
SYSCLK
VINL1
VINR1
VINL2
VINR2
VDDD
VSSD
VOUTL
VOUTR
STATUS
VREF
VDDA_ADC
VSSA_ADC
VADCP
VADCN
VDDA_DAC
VSSA_DAC
U27
LM4865MM
U28
LM4865MM
VIN-
HP
VOL
BYPASS
VO1
VO2
AVCC5;1
AGND;6
U26
MAX5413ECD
DIN
SCLK
CS
HA
WA
LA
HB
WB
LB
AVCC5;11
AGND;1
CN11
R+
R-
24-8005-002-100-867
Do not stuff
CN12
L+
L-
CN9
GND
L
R
HP-SENSE
HSJ1602-011010
HP_OUT
CN10
R-IN
R-OUT
MIC_IN
CN8
DTC143ZE-TL
TR5
TR4
Q1
2SK2980
U25
NJM2100V
VDDA;8
AGND;4
U24
NJM2100V
H8_TXD1
H8_SCK1
VOL_CS
U21
HD74LV07AT
3.3VSB;14
GND;7
OSC4
SG-8002JF-22.579200M-PCCB
F=22.579200MHZ
AC97_BIT_CLK0 2/A5
FL3
FL4
FL5
FL6
BLM18PG300SN1-D
STATUS1
STATUS0
LED1
LED2
LED3
GL100MN0MP
IR_DOUT
IR_COUT
U3
HD74LV1G08ACM
TR1
2SD2150_T100_S
IR_IN
U5
IR_DIN
U6
HD74LV1G00ACM
IR_IRQ
09
Title: MS7760CP01P/1 Circuit Diagram
Date: 7-29-2003_14:52
Sheet 9 of 12

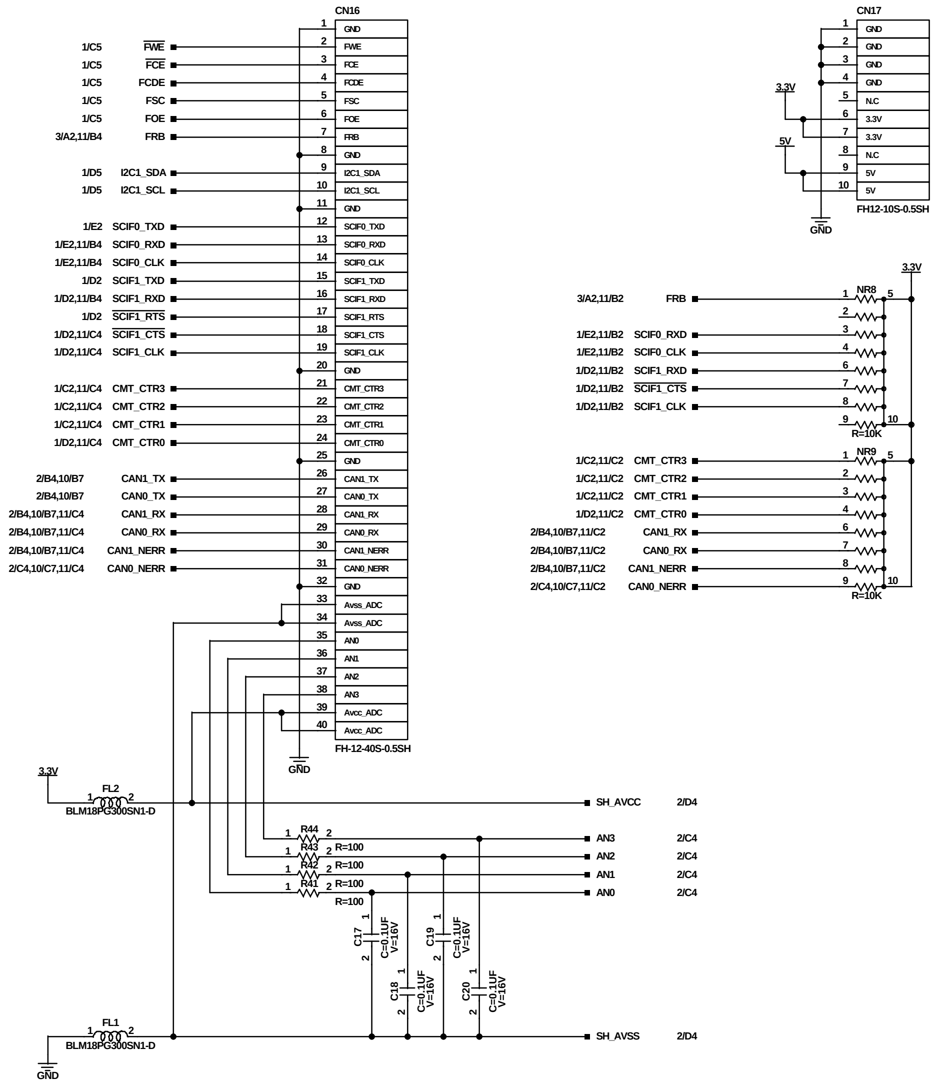
BASE BOARD INTERFACE CONNECTOR



Title: MS7760CP01P/1Circuit Diagram
Date: 7-29-2003_14:52 Sheet 10 of 12

10

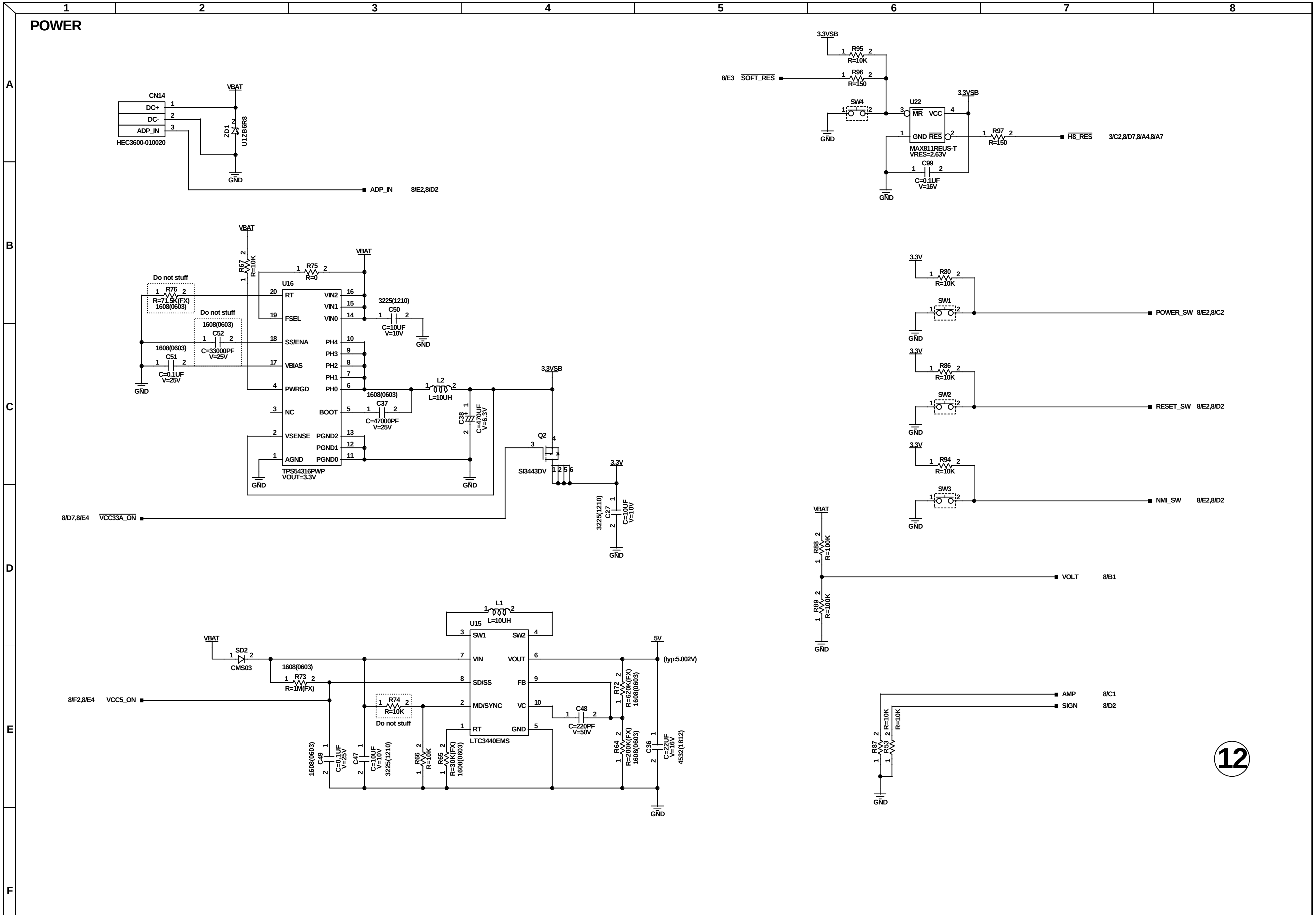
I/O PORT INTERFACE



11

Title: MS7760CP01P/1 Circuit Diagram

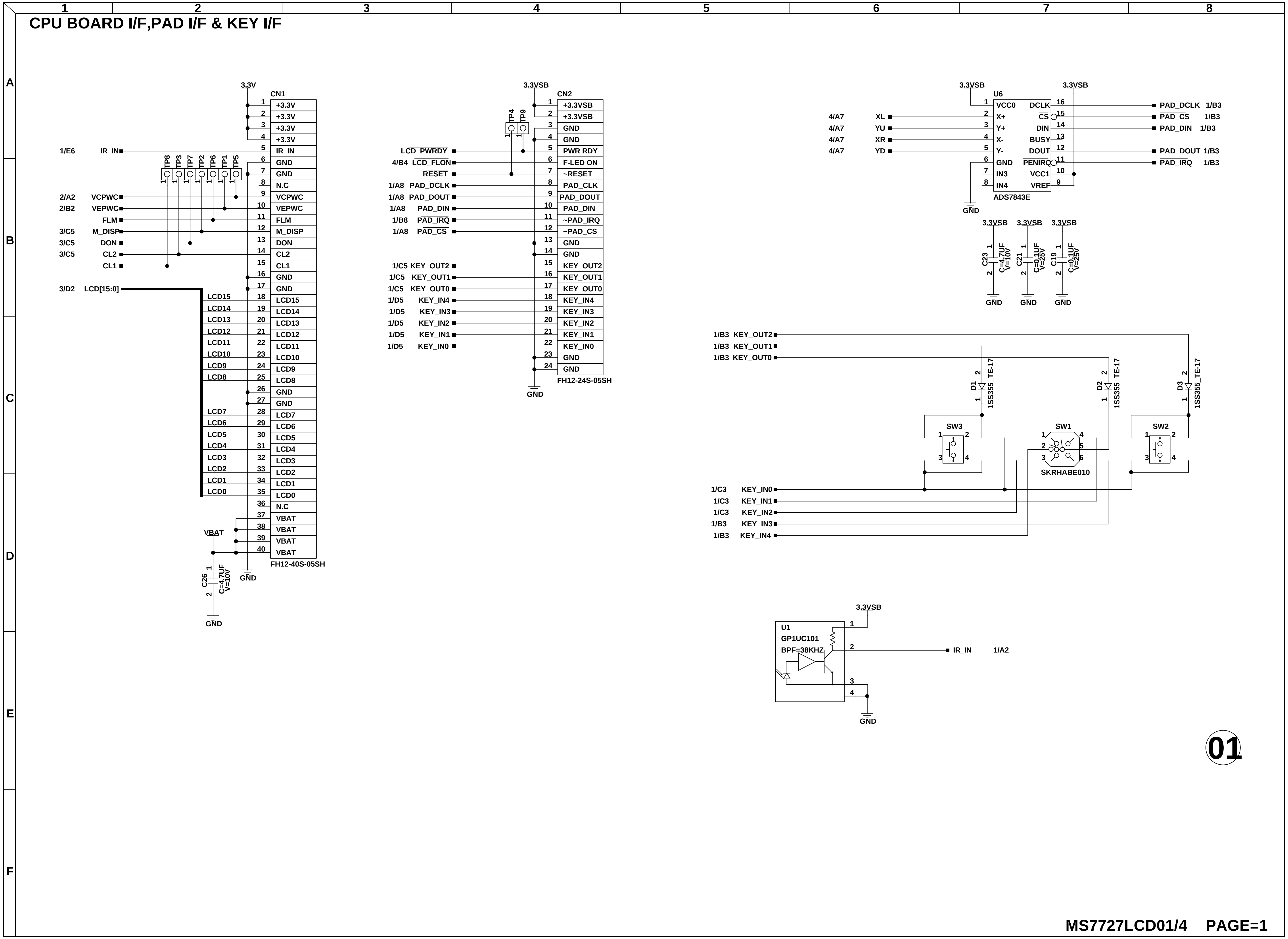
Date: 7-29-2003_14:52 | Sheet 11 of 12



Title: MS7760CP01P/1 Circuit Diagram

Date: 7-29-2003_14:52	Sheet 12 of 12

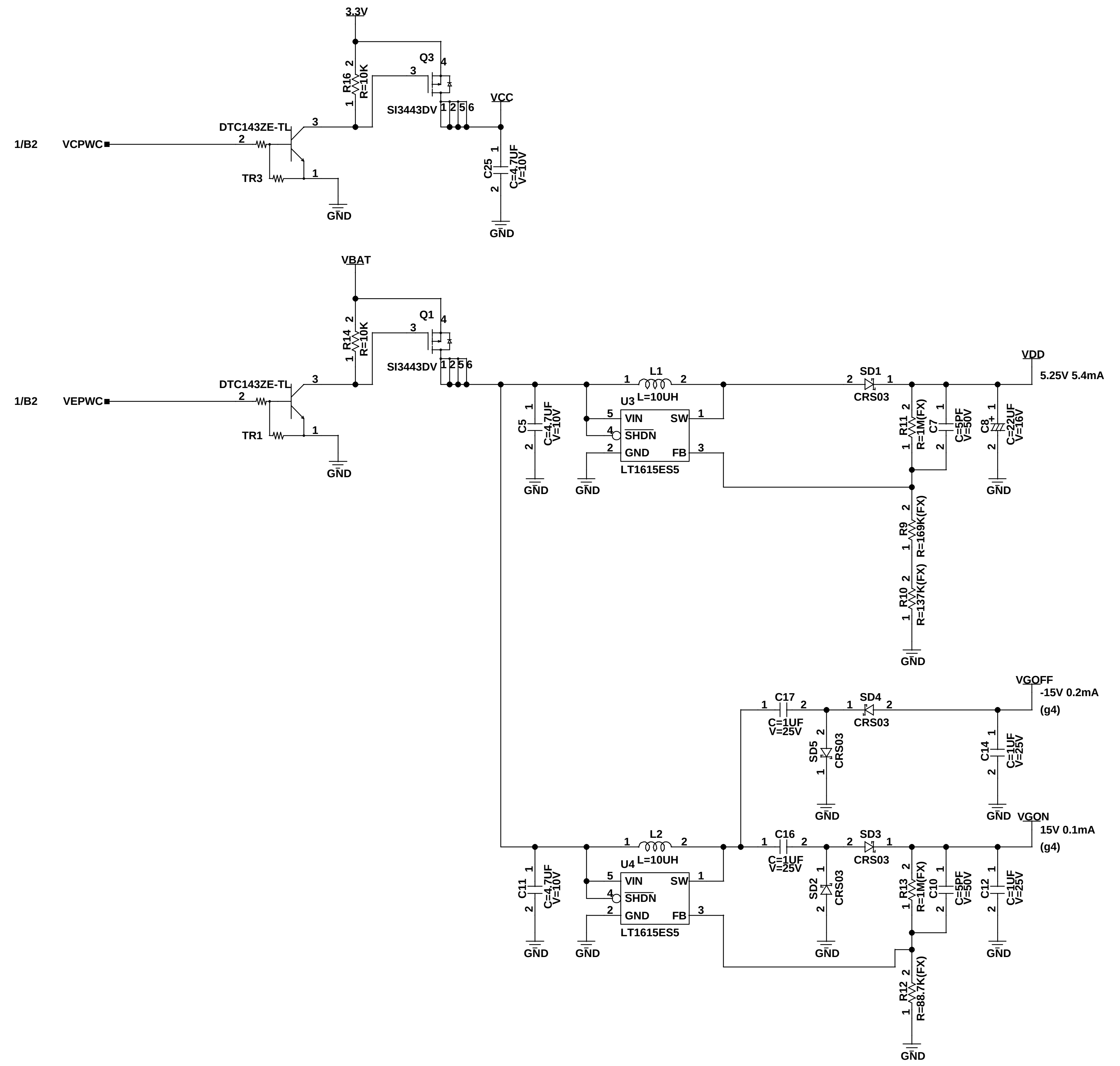
CPU BOARD I/F,PAD I/F & KEY I/F



MS7727LCD01/4 PAGE=1

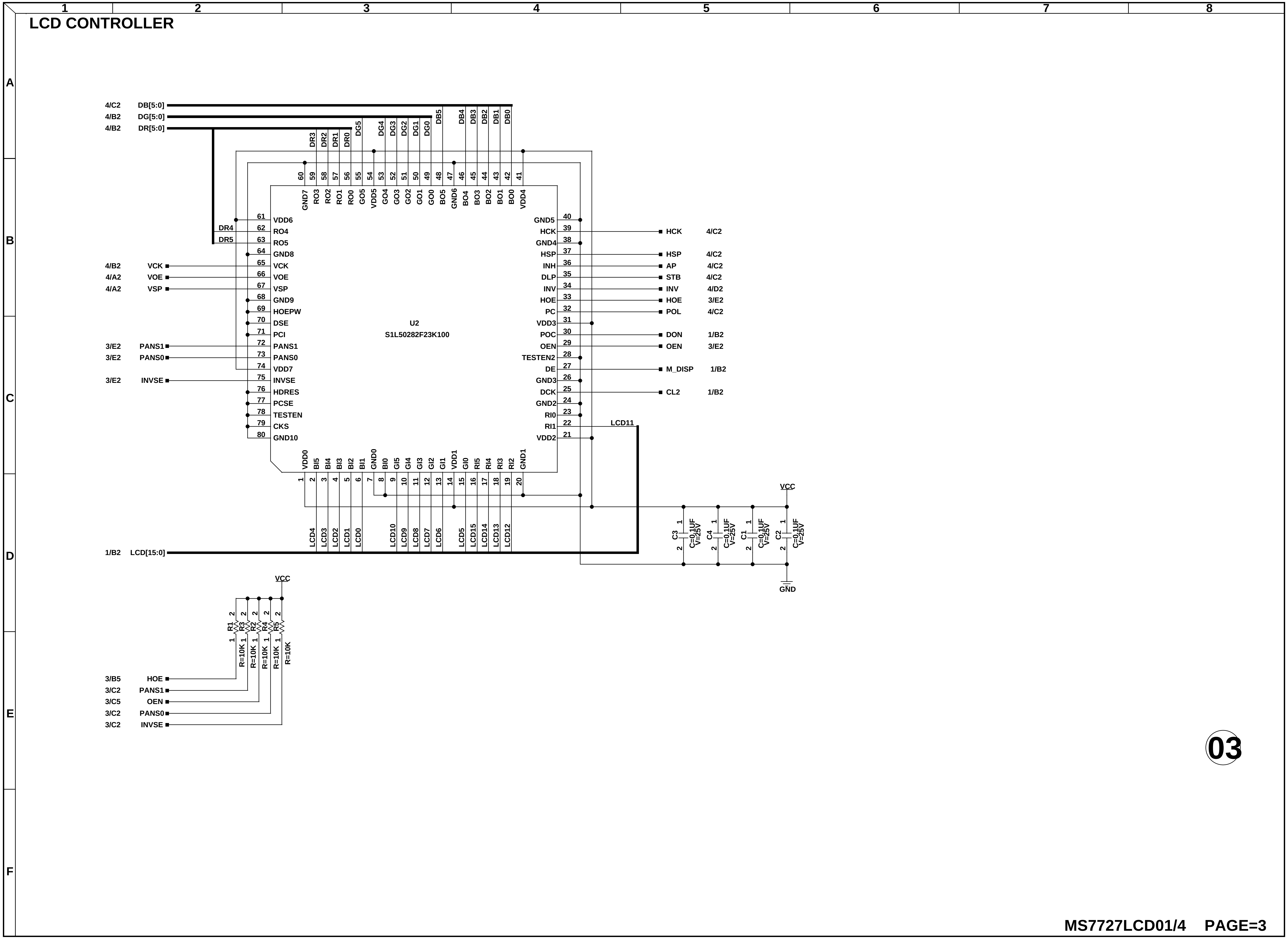
Last Update: 7-10-2002_19:56

LCD PANEL POWER



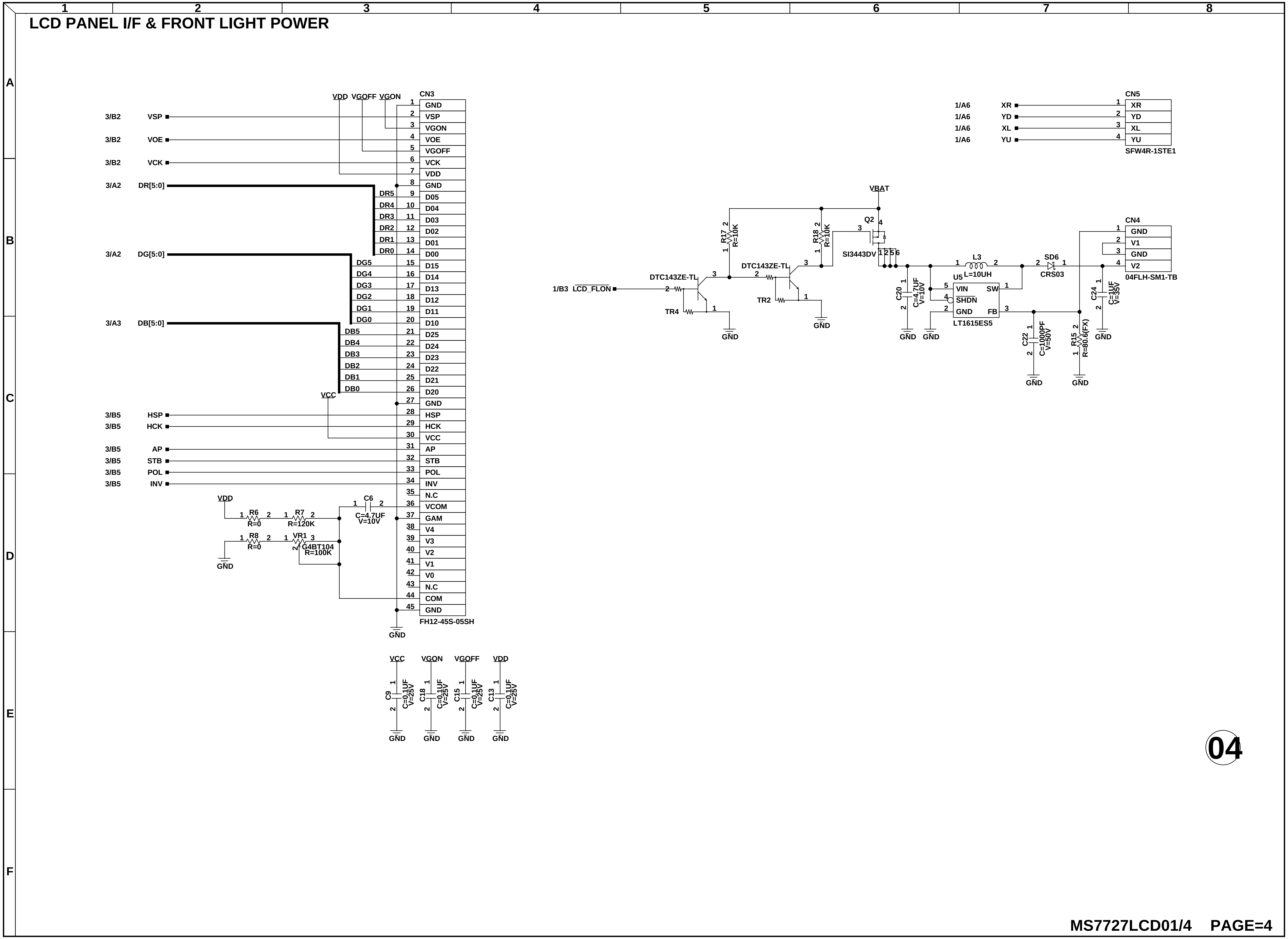
02

LCD CONTROLLER



03

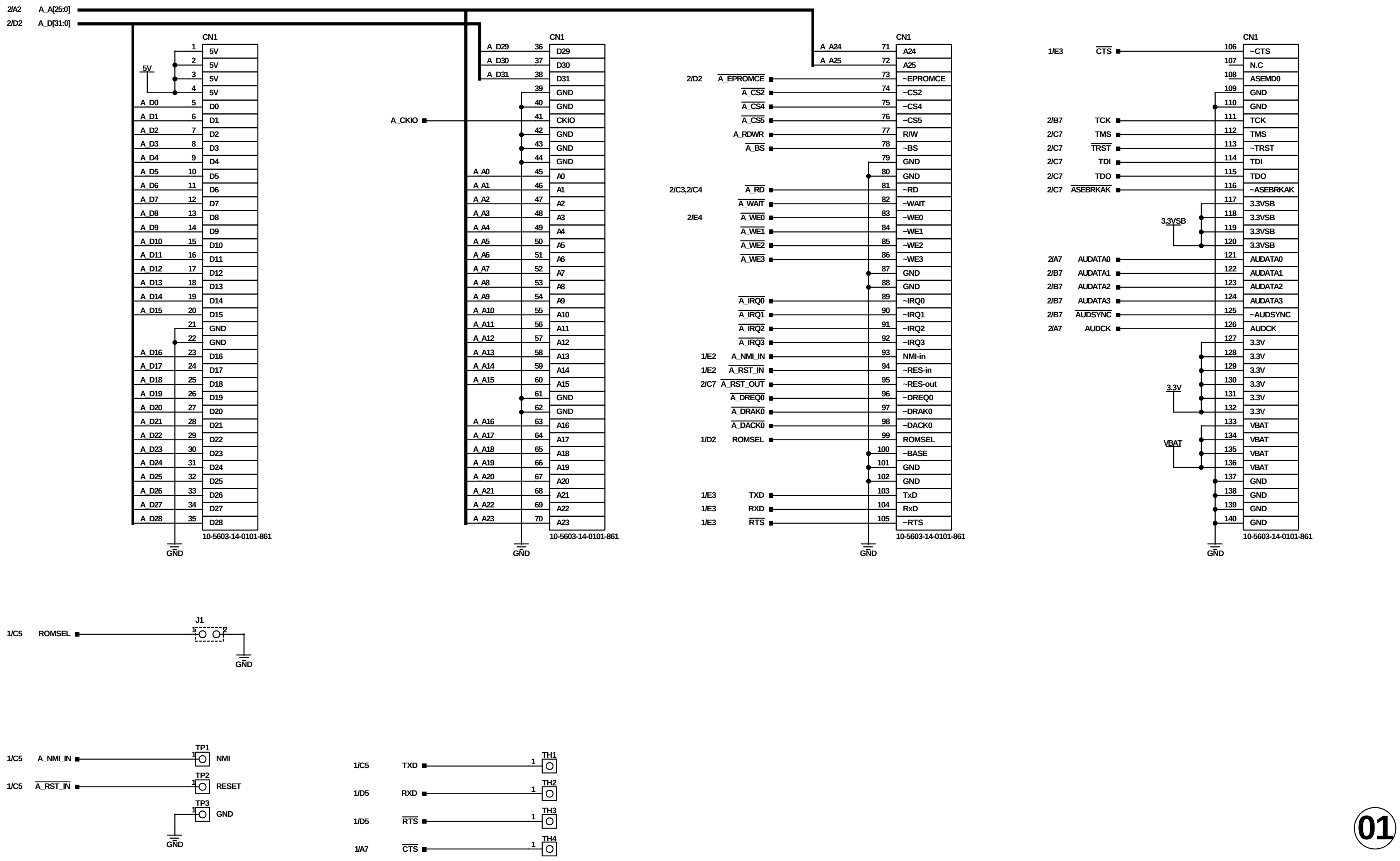
LCD PANEL I/F & FRONT LIGHT POWER



04

MS7727LCD01/4 PAGE=4

CPU BOARD INTERFACE CONNECTOR



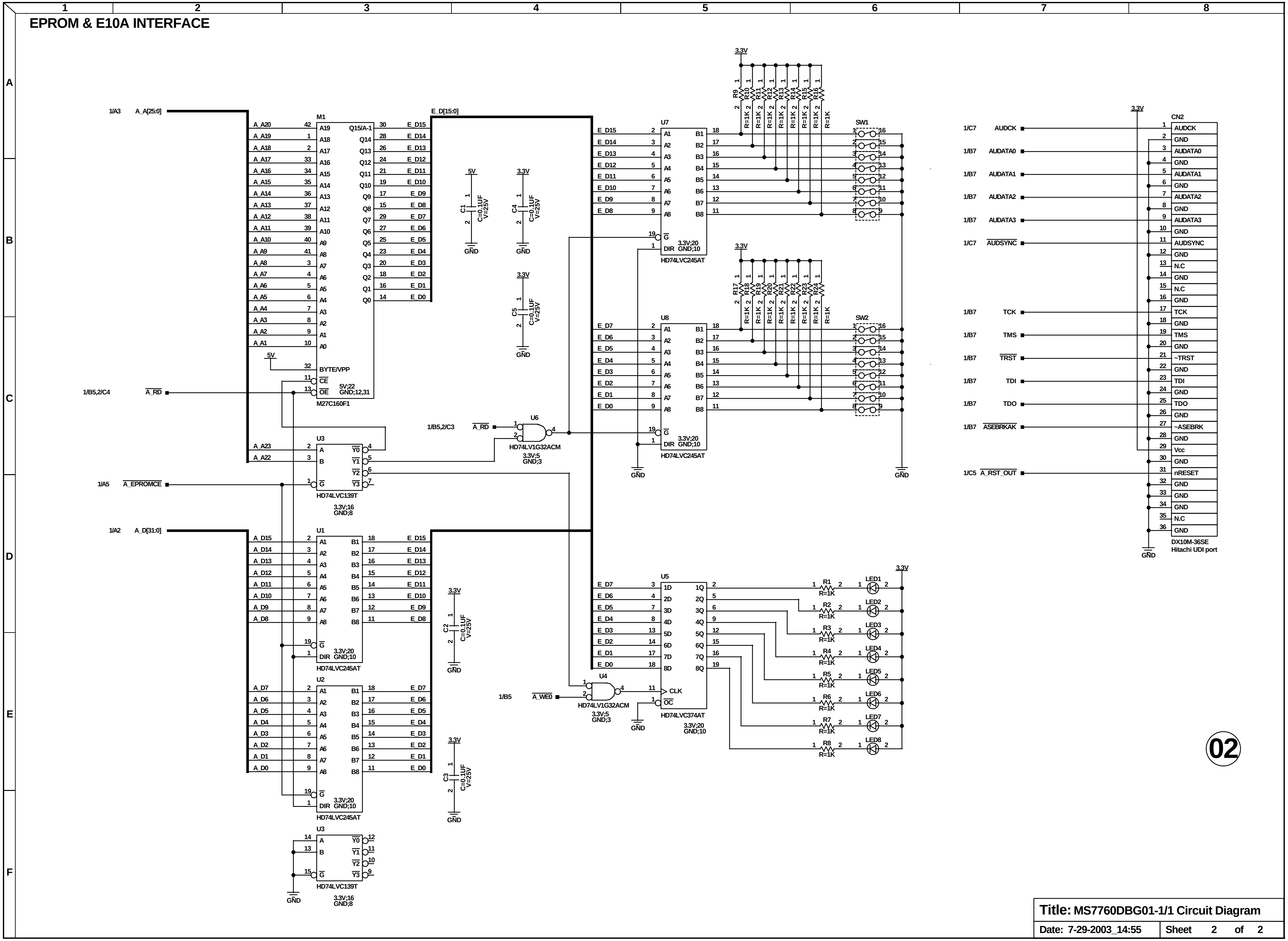
01

Title: MS7760DBG01-1/1 Circuit Diagram

Date: 7-29-2003_14:55 | Sheet 1 of 2

$1I260

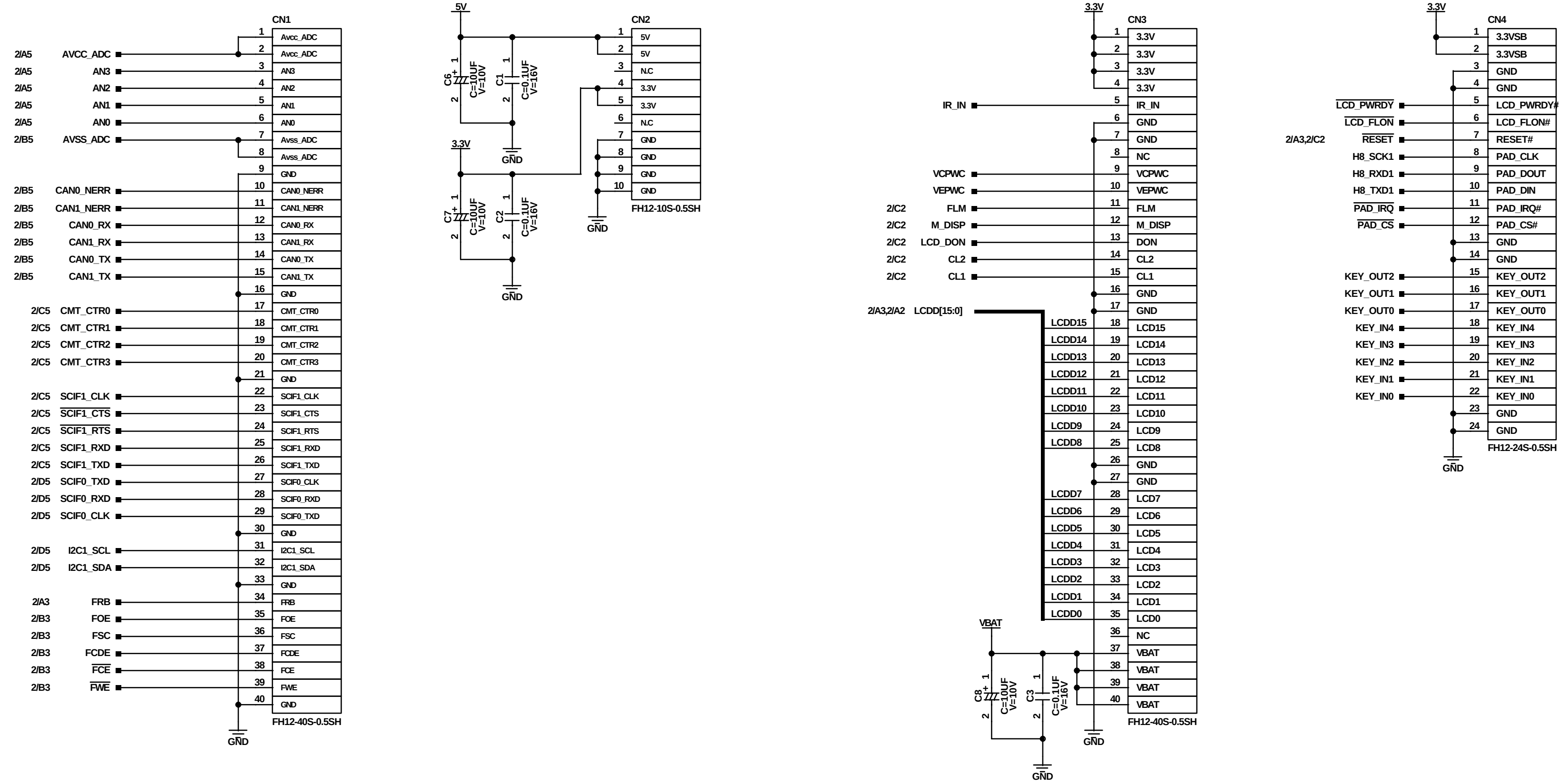
EPROM & E10A INTERFACE



Title: MS7760DBG01-1/1 Circuit Diagram

Date: 7-29-2003_14:55 | Sheet 2 of 2

CPU BOARD INTERFACE

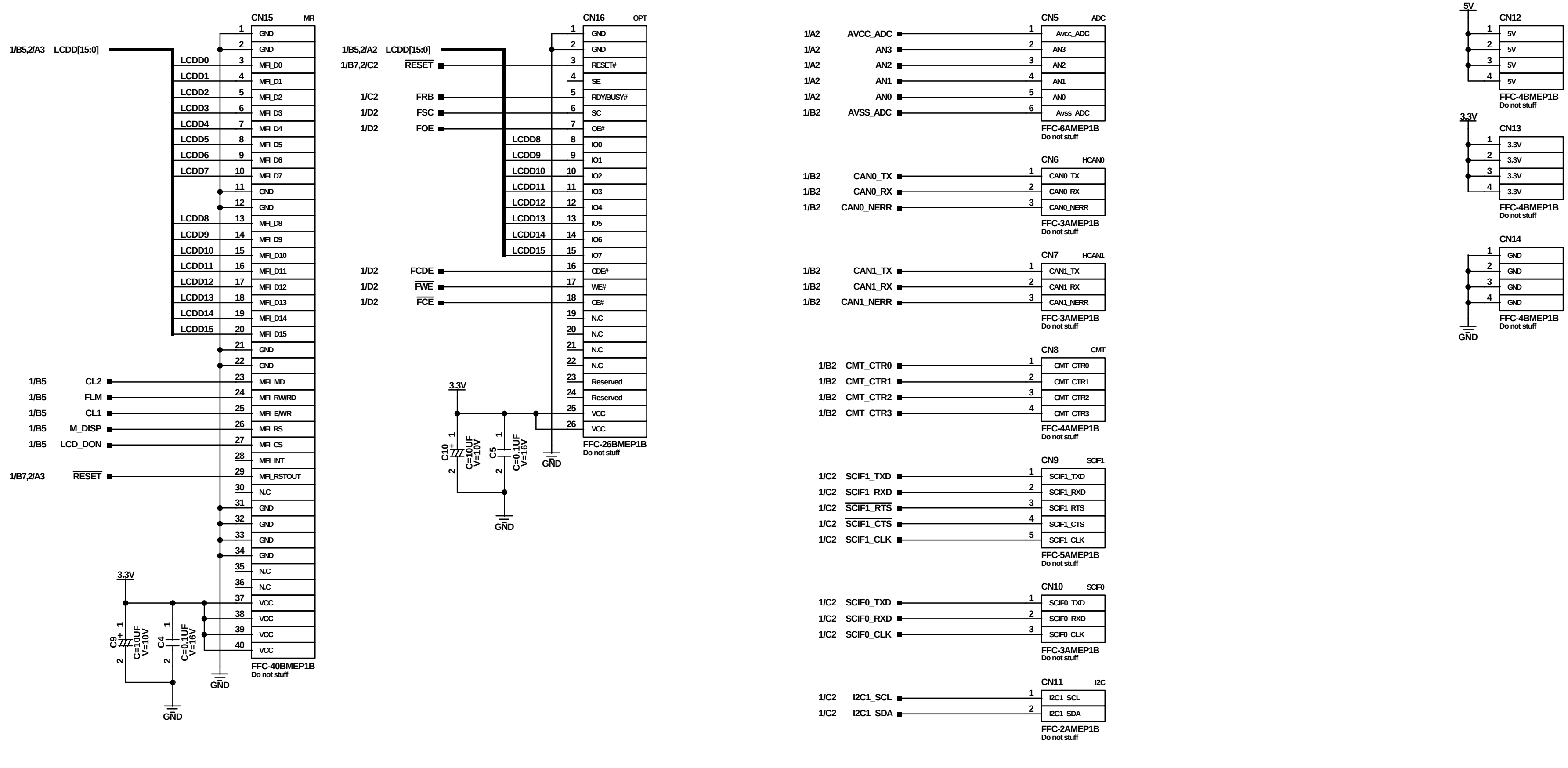


01

Title: MS7760DBG01-2/1 Circuit Diagram

Date: 7-29-2003_14:58 | Sheet 1 of 2

I/O PORT INTERFACE

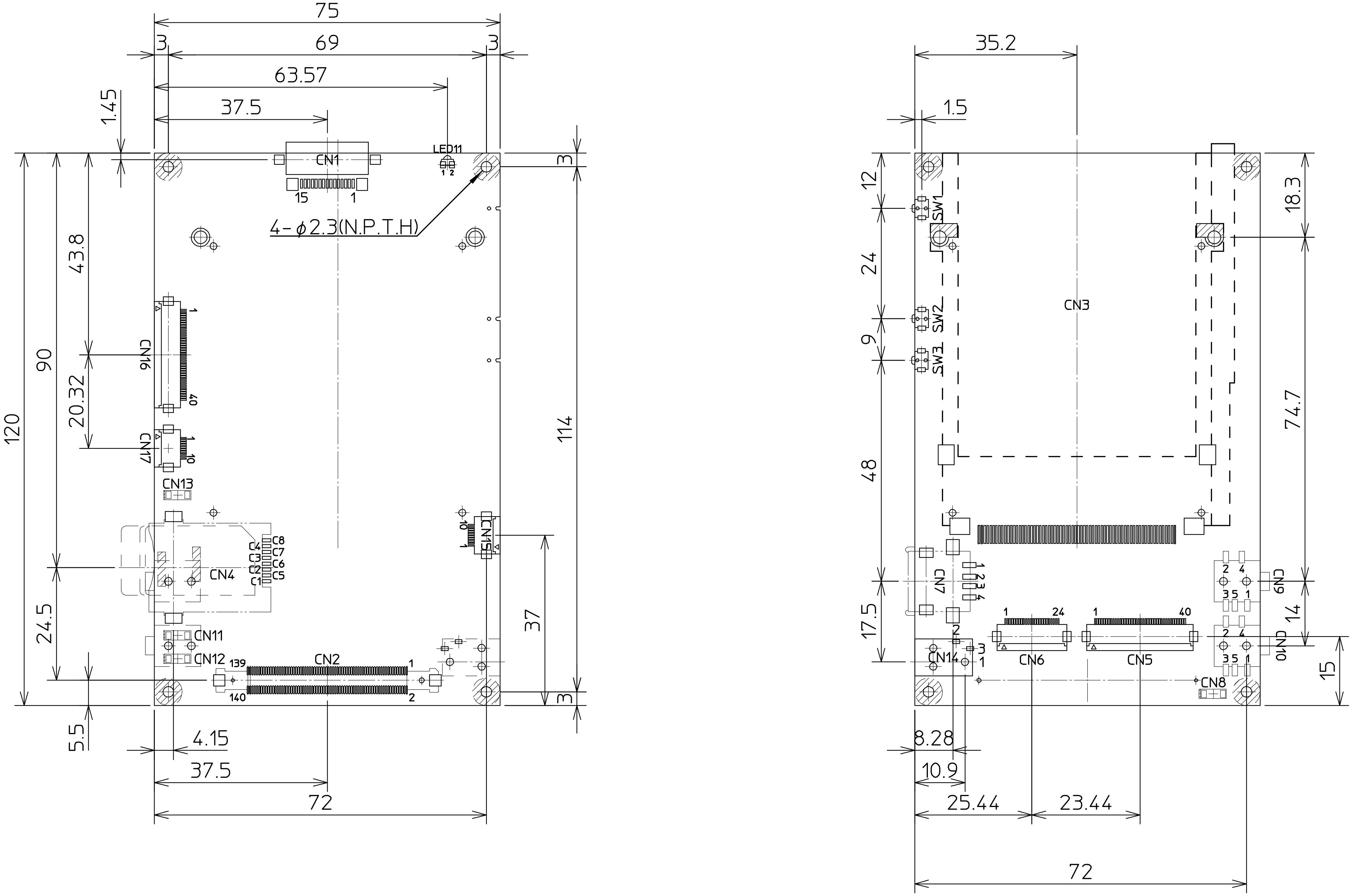


02

Title: MS7760DBG01-2/1 Circuit Diagram

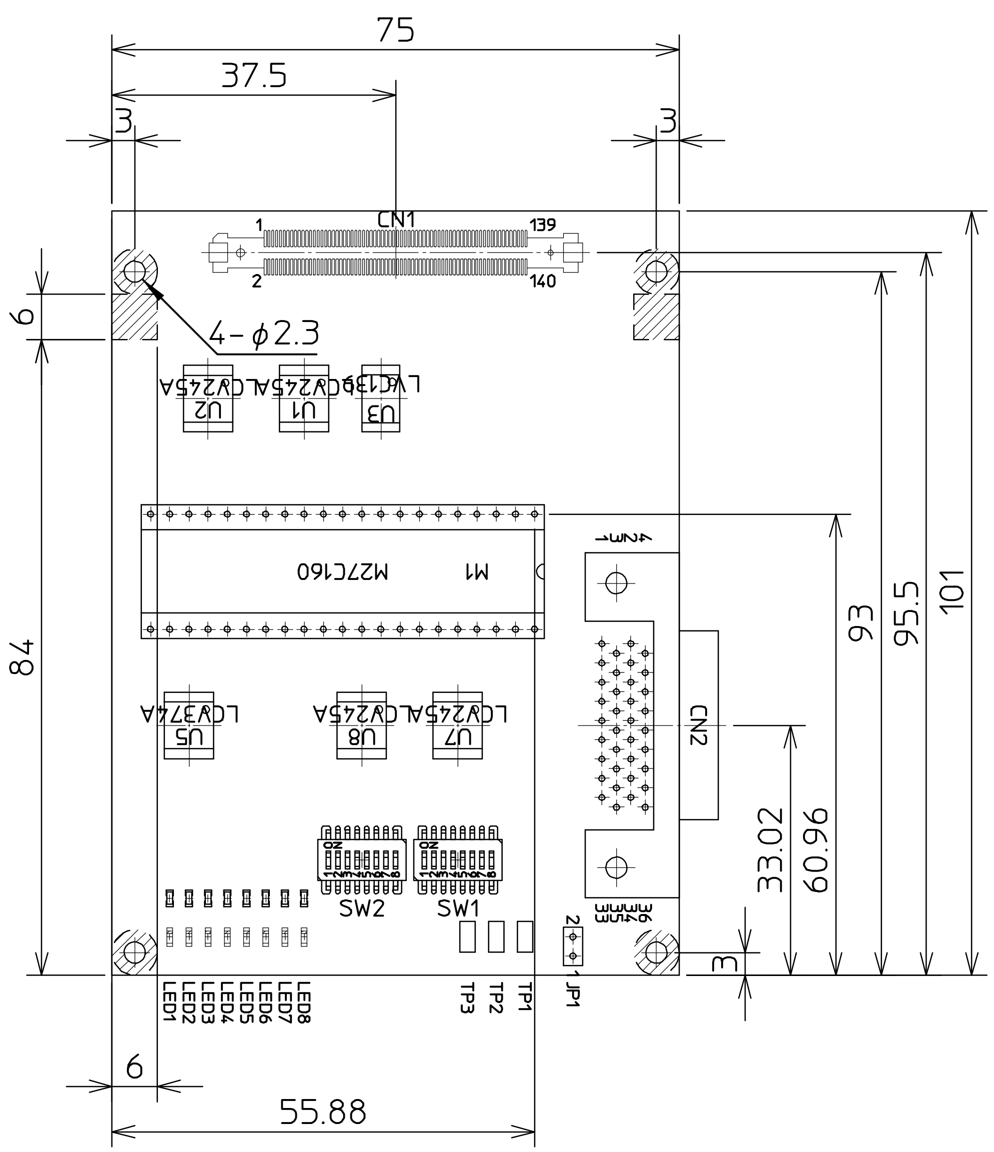
Date: 7-29-2003_14:58 | Sheet 2 of 2

[MS7760CP01]

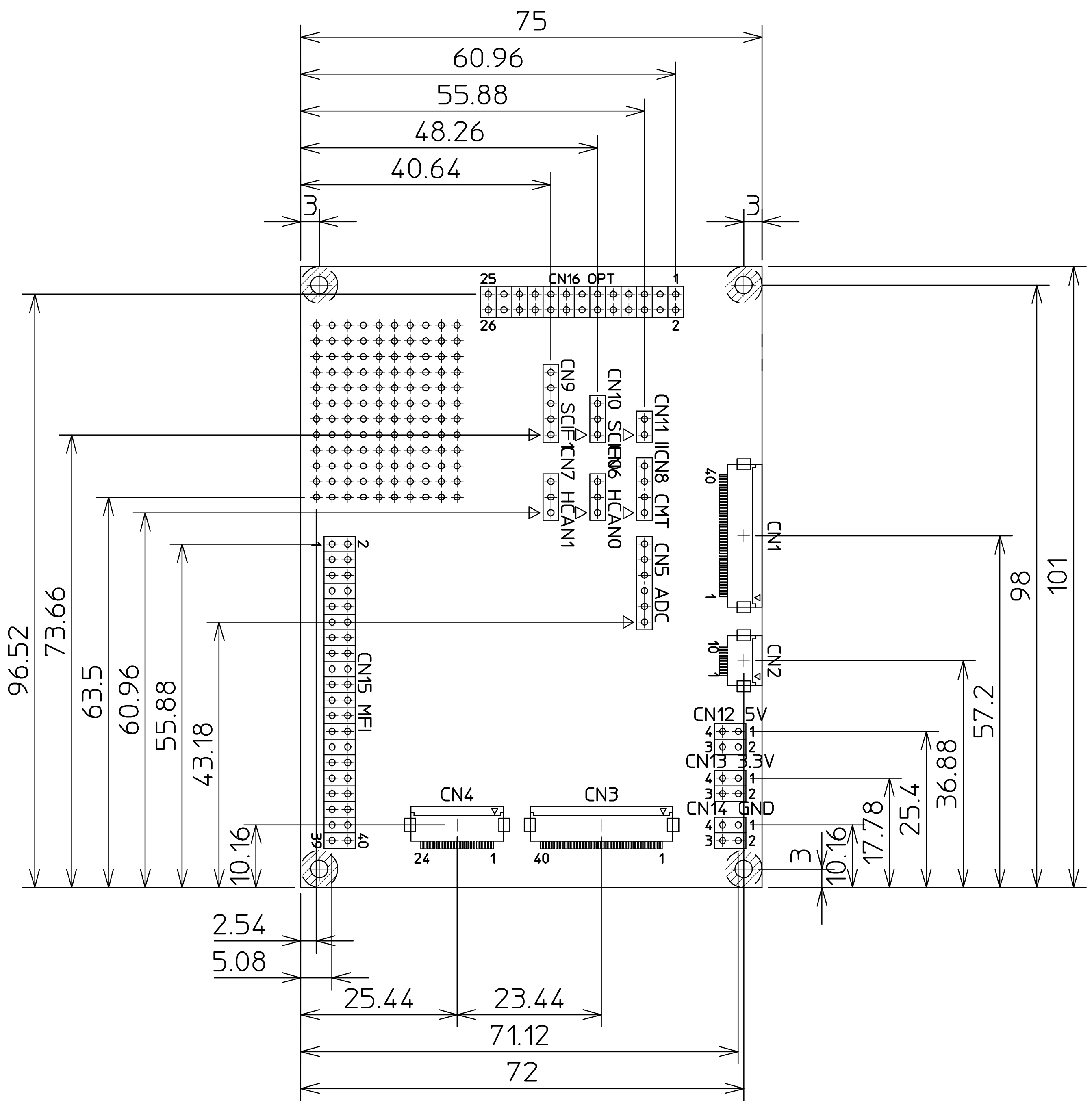


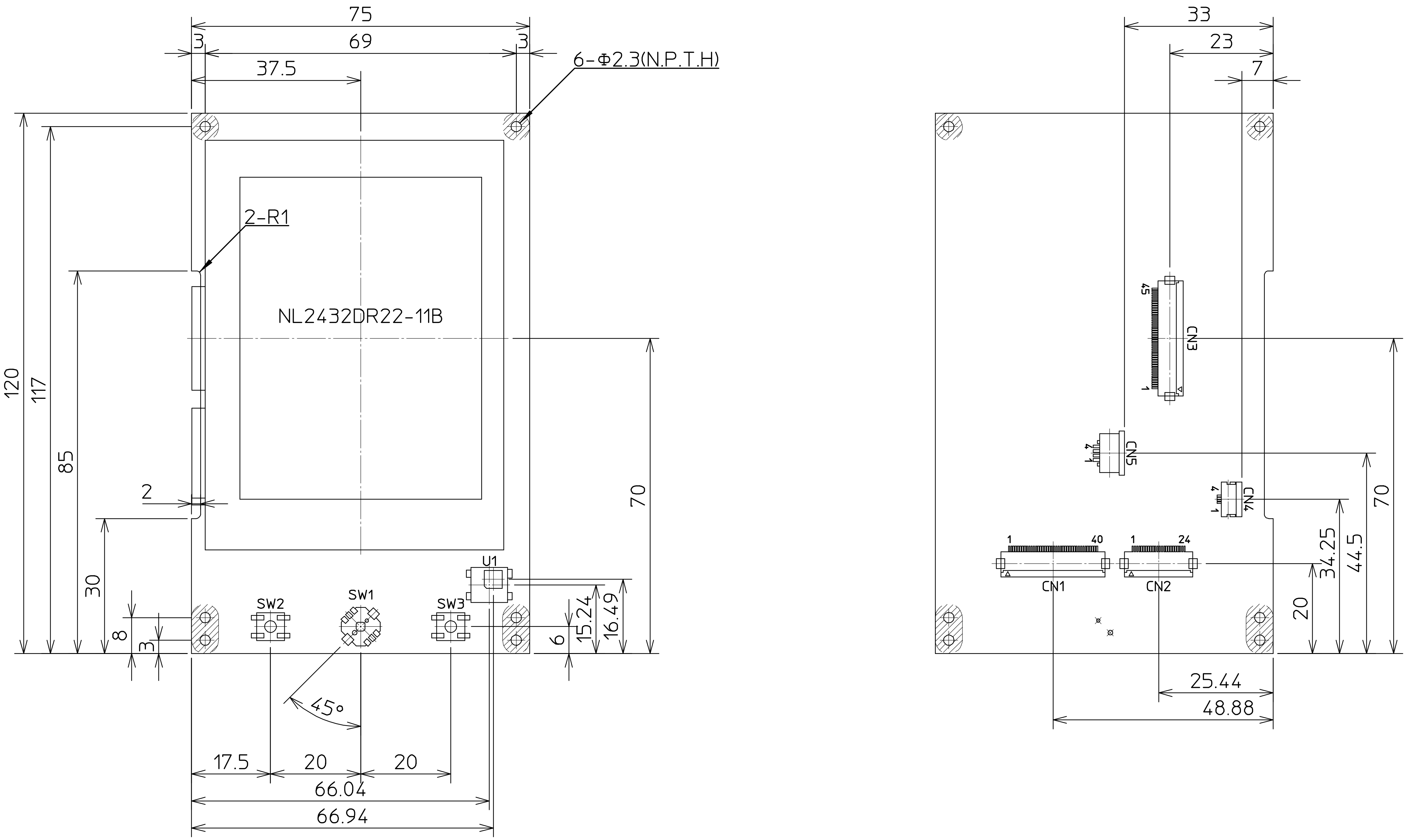
75
69
3
3
63.57
37.5
1.45
CN1
15
1
LED11
4-φ2.3(N.P.T.H)
43.8
90
120
20.32
CN16
CN17
CN13
CN4
C8
C7
C6
C5
C4
C3
C2
C1
CN15
CN11
CN12
CN2
139
140
1
2
24.5
5.5
4.15
37.5
72
114
37
3
35.2
1.5
12
SW1
24
SW2
9
SW3
CN3
48
18.3
74.7
CN7
CN9
CN10
14
17.5
CN14
CN6
CN5
24
40
CN8
15
8.28
10.9
25.44
23.44
72

MS7760DBG01-1



MS7760DBG01-2





MS7727LCD01/4基板外形寸法図

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